LEVEL

RAYTHEON **DGM** FAMILY OF DIGITAL GROUP MULTIPLEXERS

FINAL

CORADCOM-75-0036-F2

FINAL TYPE

TECHNICAL REPORT

(Volume 2 of 2: Section 3.0, 5.0, 7.0, 15.4)

DGM PROGRAM
CONTRACT NO. DAAB07-75-C-0036

FEBRUARY 1980

CDRL SEQ. NO. G037

PREPARED FOR:
UNITED STATES ARMY ELECTRONICS COMMAND
FORT MONMOUTH, NEW JERSEY

PREPARED BY:
RAYTHEON COMPANY
EQUIPMENT DIVISION
COMMUNICATIONS SYSTEM LABORATORY
SUDBURY, MASSACHUSETTS 01776

Approved for Public Release:

Distribution Unlimited

Best
Available
Copy

RAYTHEON DGM (6) FAMILY OF DIGITAL GROUP MULTIPLEXERS (DGM) Volume 2.

FINAL

FINAL TYPE

TECHNICAL REPORT

(Volume 2 of 2: Section 3.0, 5.0, 7.0, 15.4).

(9) Final rept. May 75 - Feb 80

DGM PROGRAM

CONTRACT NO. DAAB07-75-C-0036

(15)

(11) FEBRUARY 1980 (12) 145

CDRL SEQ. NO. G037

(10) William Hatton Charles Bonthank Paul Graves

PREPARED FOR:
UNITED STATES ARMY ELECTRONICS COMMAND
FORT MONMOUTH, NEW JERSEY

(18) CORADCOM (16) 1X0280 10D111

(17) 00

PREPARED BY:
RAYTHEON COMPANY
EQUIPMENT DIVISION
COMMUNICATIONS SYSTEM LABORATORY
SUDBURY, MASSACHUSETTS 01776

(19) 75-0036-F2

407751

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont.)

TABLE OF CONTENTS (Cont.)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont.)

LIST OF ILLUSTRATIONS (Cont.)

LIST OF ILLUSTRATIONS (Cont.)

LIST OF TABLES

LIST OF TABLES (Cont.)

SECTION 3
LGM

The Loop Group Multiplexer (LGM) is used in tactical communications shelters and vans. Its primary function is the time division multiplexing of up to sixteen (16) conditioned diphase loops into a loop group and the time division demultiplexing of a digital group into its constituent channels. One channel of the loop group is allocated for overhead (non-traffic) functions, such as the framing pattern and telemetering data for SYSCON. Local access to the overhead channel's SYSCON telemetry subchannel is provided at the LGM.

The conditioned diphase interface at the loopside is provided by a Loop Modem element which operates at a 32 or 16 kb/s rates. The Loop Modem elements primary function is to transmit and receive conditioned diphase signals on the cable connecting it to a DSVT or another digital subscriber set which has the same functional and interface requirements of a DSVT. In addition, the Loop Modem element provides DC power to the DSVT for common battery operation. Two Loop Modem elements are packaged on a single P.C.B.

The Group Framing and Synchronization element generates and detects the frame synchronization patterns required to maintain link synchronization. Frame sync acquisition is initiated when the out of sync condition is detected. In addition, the Group Framing and Synchronization element commands the Trunk Encryption Device (TED) to resynchronize when required during frame synchronization acquisition when a TED is used.

The group interface provides a full duplex digital group consisting of balanced NRZ data which may be connected to a TED, GM, TGM, MGM or Low Speed CDM.

Generation of the internal timing signals required by the LGM is performed by the Clock and Timing Generator element. The LGM operates on reference timing at the group rate from either an external source or from the received group clock.

The LGM design also includes BITE, for O&M support.

The LGM DC power is obtained from its Power Supply element which operates from AC or DC primary power sources.

3.1 DESIGN GOALS AND REQUIREMENTS

The LGM function requirements are summarized in Table 3-1.

A major design objective in the LGM was directed toward reducing the number of printed circuit boards (P.C.B.'s) required to meet the functional requirements for the LGM and to minimize the input power required.

This objective was of major importance in view of the savings in combining the Loop Modem (LM) unit with the Loop Group Multiplexer (LGM) unit.

To this end, by optimizing the design and partitioning of circuits, a design has been achieved which significantly reduces the P.C.B. card types and thus, permitted the Loop Group Multiplexer (LGM) and the Loop Modem (LM) to be combined into a single unit.

3.2 DESIGN APPROACH

3.2.1 Summary

There are a number of basic design approaches which the subcontractor used throughout the design to optimize commonality with the Raytheon units. Basic design approaches were as follows.

TABLE 3-1. FUNCTIONAL REQUIREMENTS - LOOP GROUP MULTIPLEXER (LGM)

Definition: The LGM shall multiplex up to 16 conditioned diphase channels into a single digital time division multiplexed loop group. One of the channels shall be an overhead channel for framing and telemetry.

	Loop Side		Group Side
Type of Channels:	4 wire full duplex		Same
Number of Channels:	7, 8, 15, or 16		8, 9, 16, or 18
Bit Rate:	32/16/kb/s		128, 144, 256 or 288 kb/s at 16 kb/s Loop Rate 256, 288, 512, or 576 kb/s at 32 kb/s Loop Rate
Modulation:	Conditioned Diphase		NRZ, balanced
Used With:	DSVT		TED or GM
Power Feed:	DSVT per TT-A3-9002-0017		
Impedance:	125 $\pm$10% Return Loss > 26 dB in the band from 8 to 56 KHz		
Crypto Interface:			TED
Timing:			Station Clock/Receive Group Clock
Modularity:	Loops	16 kb/s Loops	32 kb/s Loops
	7	128	256
	8	144	288
	15	256	512
	16	288	576
Overhead Channel Structure:	Eight subchannels, one channel is framing, a second is telemetry		
Telemetry Sub-channel Access:	Access shall be provided to the LGM 2 kb/s telemetry subchannel		
Size:	8.5" H x 12" D x 19" - Rack Mount		
Input Power:	190 watts maximum		
Type of Power:	115 VAC $\pm$10%, 50 to 400 Hz		
Weight:	17 KG		
BITE:	Power Monitor/Fault Isolation Loss of Sync Channel Failure		
Reliability:	3,000 HR-MTBF		

a. The extensive use of C-MOS devices. An extensive trade off study was performed on the use of Low Power Schottky devices versus C-MOS. The results of this study showed that, on the average, a five to one power savings could be achieved by using C-MOS. This significant power savings was achievable since the speeds at which most of the circuits operated were below 1 MHz. Low Power Schottky devices are used when operating at higher frequencies.

b. Common printed circuit boards are used in the field and shelter units. Since these are identical function; i.e., framing and synchronization, to be performed in both the shelter and field units, identical cards are used to perform these common functions. Variations in specific requirements; i.e., group output rates, MUX/DEMUX sequences are selectable by toggle switches mounted to the P.C.B.'s. Back plane wiring is used to insure that illegal sequences cannot be selected when a common card is placed in a unit.

c. Minimized the design of the loop modem circuit so that two loop modems were packaged on a single P.C.B.

d. Designed the Power Supply so that common circuit designs are used in the field and shelter units.

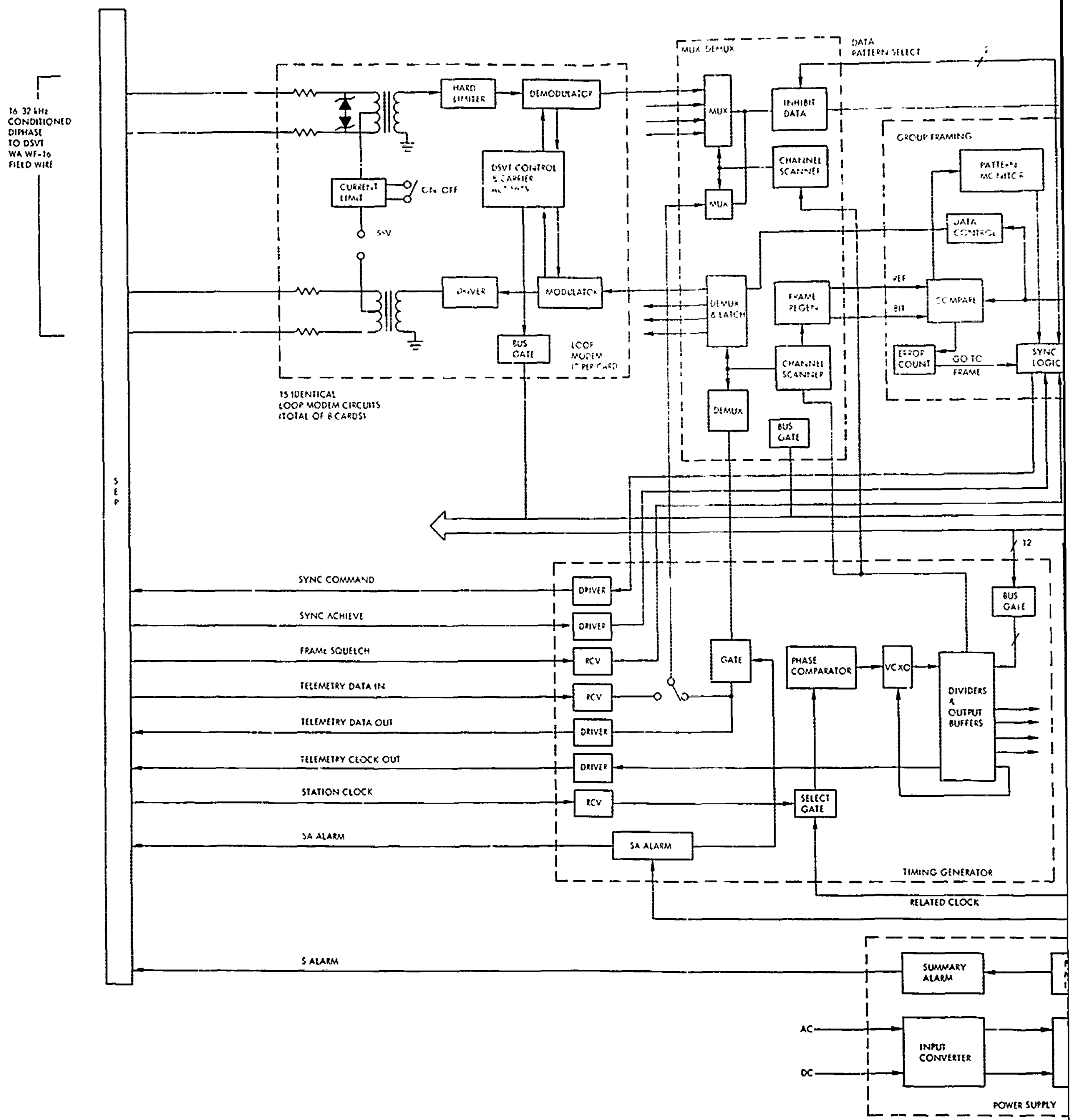
e. Designed the loop modem P.C.B.'s so that they are completely interchangeable with the loop modem P.C.B.'s used in the field units.

f. Designed a Clock and Timing P.C.B. which is interchangeable with the Clock and Timing P.C.B.'s located in the RMC and RLGM units.

g. Mechanical design approaches are discussed in Paragraph 15.4 of this volume.

3.2.2 Detailed Electrical Design for the LGM

A detailed block diagram of the LGM is shown in Figure 3-1. The LGM time division multiplexes up to eighteen (18) digital channels into a single digital time division multiplexed loop group. One of the eighteen (18) channels is an overhead channel which transmits framing and SYSCON telemetry data. The LGM contains sixteen (16) conditioned diphase loop modems. Two modems are packaged on a single P.C.B. The loop modems accept baseband digital loop


16 32 kHz CONDITIONED DIPHASE TO DSVT WA WF-16 FIELD WIRE
SEP
HARD LIMITER
DEMODULATOR
DSVT CONTROL
CURRENT LIMIT
ON OFF
DRIVER
MODULATOR
BUS GATE
LOOP MODEM
15 IDENTICAL LOOP MODEM CIRCUITS (TOTAL OF 8 CARDS)
MUX DEMUX
DATA PATTERN SELECT
MUX
INHIBIT DATA
CHANNEL SCANNER
DEMUX & LATCH
FRAME REGEN
DEMUX
GROUP FRAMING
PATTERN MONITOR
DATA CONTROL
COMPARE
ERROR COUNT
GO TO FRAME
SYNC LOGIC
12
SYNC COMMAND
SYNC ACHIEVE
FRAME SQUELCH
TELEMETRY DATA IN
TELEMETRY DATA OUT
TELEMETRY CLOCK OUT
STATION CLOCK
SA ALARM
DRIVER
RCV
GATE
PHASE COMPARATOR
VCXO
DIVIDERS & OUTPUT BUFFERS
SELECT GATE
TIMING GENERATOR
RELATED CLOCK
S ALARM
SUMMARY ALARM
AC
DC
INPUT CONVERTER
POWER SUPPLY

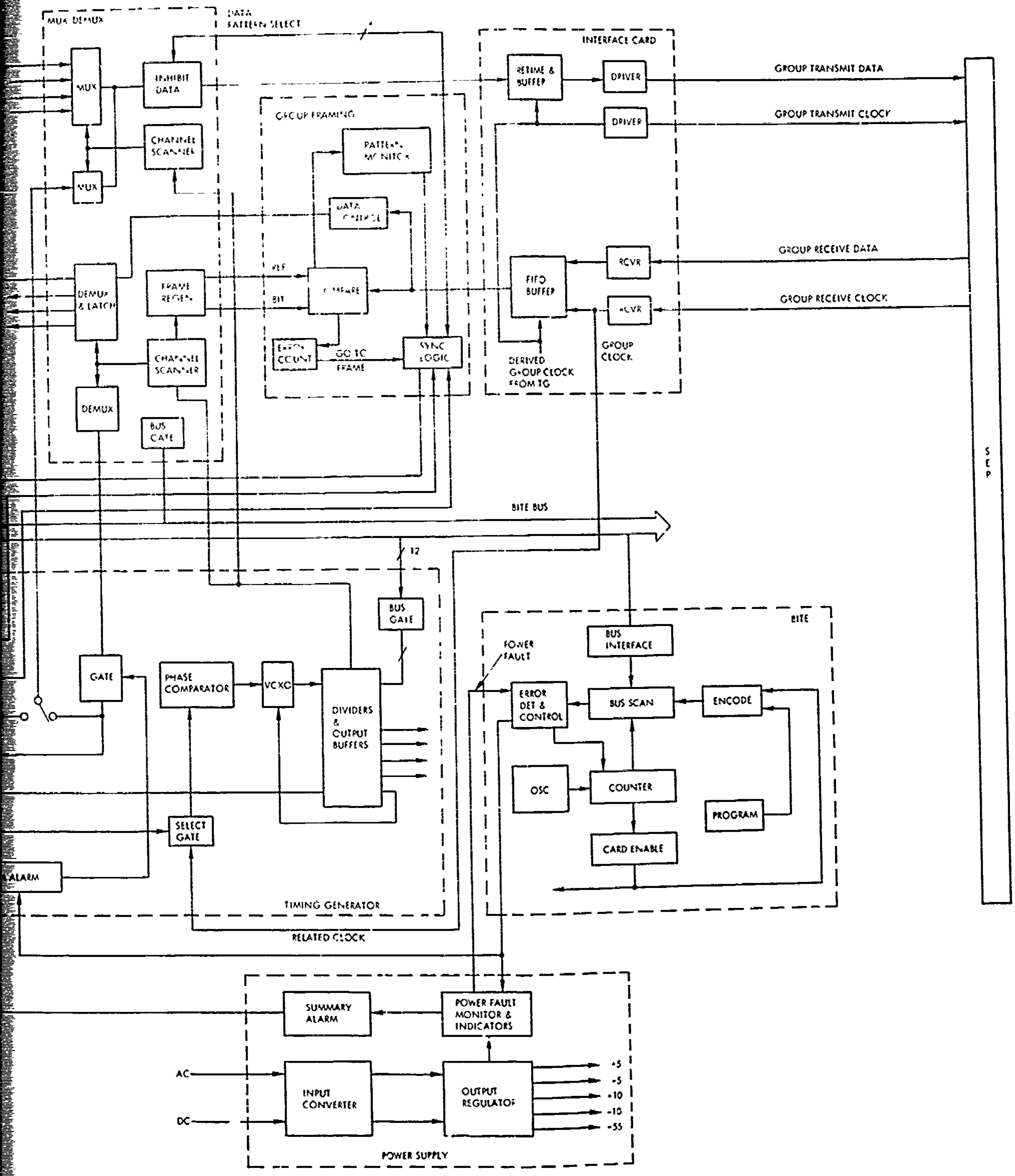


Figure 3-1. LGM Block Diagram

2

signals from the MUX/DEMUX P.C.B. and modulate/demodulate the loop data for transmission to digital voice subscriber terminals via telephone (WF-16) cable. The modems also provide phantom loop power over this same cable to power the DSVT operating in a common battery mode. A switch is provided on each loop modem to control the power (on/off) to each DSVT. Second level EMP protection circuits are located on each loop modem.

The Loop Modems NRZ baseband data is passed to the MUX/DEMUX card where it is multiplexed with the overhead channel containing the SYSCON sub-channel. The resulting bit interlaced data stream is sent to the Group Framing Unit where the data is gated to the output group data interface under control of the Synchronizer section of the Group Framing Unit. The output data stream is buffered and converted to a balanced interface on the interface card before appearing at the external connector interface.

The group data input is converted from a balanced signal to C-MOS (Interface Card) and inputted to a ±8 bit FIFO. The re-timed data is then connected to the frame regenerator portion of the Group Framing Unit. The frame regenerator is a counter whose output (frame pattern) is aligned in phase with the incoming frame pattern in the data. The frame reference is used to properly phase the MUX DEMUX circuitry. The demultiplexed data channels are buffered. and applied to each loop via the Loop Modems. A multi-pin connector is used at the rear of the LGM unit for the loop signals.

The Timing Generator locks an internal oscillator to an external station clock which is applied as a balanced line input at the group bit rate. Toggle switches located on the Timing Generator P.C.B. are used to program the proper output clock rate: the switch outputs are also used to program the MUX/DEMUX card.

A switch is also provided on the Timing Generator P.C.B. to provide a loop-back capability for the SYSCON telemetry sub-channel. This sub-channel may be looped back either internally - output of the demultiplexer connected directly to the multiplexer or externally via the SYSCON external connections.

n addition, a summary BITE alarm (SA) will cause ZERO's to be inserted on the receive side of the telemetry subchannel.

The BITE card monitors key signal status on each P.C.B. within the LGM. These signals are transmitted to the BITE P.C.B. over a sixteen (16) bit buss. The BITE P.C.B. sequentially addresses each P.C.B. within the unit and determines whether all the "key" signals are present. If not, a one second delay is started and the signals tested again. If after the one second delay, the fault persists, a summary error flag is raised. This flag causes the S and the SA (depending upon the fault) alarm to be energized. An LED located on the defective P.C.B. will then be illuminated along with the Summary Error indicator located on the front panel of the power supply. In the event that the BITE has detected a fault which could be caused by an external error (interface unit), the LED located on the BITE P.C.B. will illuminate. The fault LED located on the BITE P.C.B. is used to indicate external errors only.

The LGM power supply operates from 120 VAC, 50 to 400 HZ single phase power. The power supply outputs are ±10 VDC, ±5 VDC, and +55 VDC. The 5 and 10 VDC voltages are used internally to power the LGM P.C.B.'s. The +55 Volt output is used for powering the DSVT's via phantom loops. The Power Supply contains fault monitoring circuits which monitor the status of each output voltage. When an out-of-tolerance indication is detected, the Power-out-of Tolerance and Summary Fault indicators are illuminated.

3.2.3 Interface Description

The LGM interface requirements are summarized in Table 3-2 and are described in the following sections.

3.2.3.1 Loop Interface (J1 and J2)

The LGM loop interface provides connections for 7, 8, 15 or 16 full duplex digital loops. Each loop interface shall consist of transmit loop data and receive loop data. The signals are conditioned diphase modulated signals. he signal rates are 16 kb/s or 32 kb/s. The signal lines are balanced.

TABLE 3-2. LGM INTERFACE SPECIFICATION SUMMARY

Connector	Function	Signal Rate/ Frequency	Signal/Line Characteristics	Type of Cable Connection Required	Number of Wires in Connector
J1	• Transmit and Receive Loop Data (Line Side) - Channels 1 through 8	16 or 32 kb/s	Conditioned Diphase	8 individual quads - each quad shielded	40
J2	• Transmit and Receive Loop Data (Line Side) - Channels 9 through 16	16 or 32 kb/s	Conditioned Diphase	8 individual quads - each quad shielded	40
J3	• Transmit group data • Receive group data • Transmit group clock • Receive group clock	256, 288, 512 or 576 kb/s @ 32 kb/s loop rate or 128, 144, 256 or 288 kb/s @ 16 kb/s loop rate	NRZ, Balanced	4 individual shielded twisted pairs	12
J4	• Sync command • Sync achieve	-10 μs DC level DC level	Balanced Unbalanced	2 individual shielded twisted pairs	6
J5	• Station clock	Group Rate	Balanced square wave	1 shielded twisted pair	3
J6	• Telemetry data out • Telemetry data in • Telemetry clock out • Frame squelch (in) • SA Alarm • Summary Alarm	2 kb/s 2 kb/s 2 kb/s DC Contact Closure Contact Closure	NRZ, Balanced NRZ. Balanced Balanced Square wave TTL compatible ALM = Close Contact ALM = Close Contact	6 individual twisted pairs with overall shield	13
J7	• Prime power	AC 50, 60, or 400 Hz		3 conductors	3

DSVT power feed is provided on each line via a phantom loop. Two multi-pin connectors are used for these signals.

3.2.3.2 Group Interface (J3)

The group interface interfaces with a full duplex digital group which connects to a Group Modem or TED. The group interface consists of transmit group data and receive group data; transmit group clock and receive group clock. The signals will be NRZ. The line is balanced. The signal bit rates are 256, 288, 512 or 576 kb/s for loop data rates of 32 kb/s and 128, 144, 256, or 288 for loop data rates of 16 kb/s. A single connector is provided for these signals. When connecting to this interface, a cable consisting of shielded twisted pair should be used.

Cabling between the LGM and GM and between the LGM and the TED will be made from this common connector located on the LGM. It should be noted that when the LGM is connected to the TED, the TED control signals, Resync Command and Resync Achieved, are terminated in a separate LGM connector. Since these signals must be combined with other TED signals, a junction box of some kind must be provided outside the LGM unit. This junction box is not supplied.

3.2.3.3 TED Control Lines (J4)

A common connector is provided to carry the two black TED control signals required for TED synchronization. These signals are SYNC ACHIEVE and SYNC COMMAND. The interface cable connecting to this connector must be shielded twisted pair.

3.2.3.4 Station Clock (J5)

The LGM will accept a station clock input. The frequency of the clock is at the group bit rate.

3.2.3.5 TELEMETRY/SQUELCH/ALARM Signals (J6)

A common connector is provided to carry the SYSCON TELEMETRY signals (2 kb/s), the FRAME SQUELCH signal and contact closures for the ALARM outputs. A switch is provided in the LGM which will internally connect the SYSCON Telemetry output to the SYSCON TELEMETRY source. The frame squelch (inhibit) is a DC input. When active, this signal inhibits frame search within the LGM.

3.2.2.6 Prime Power (J7)

A common connector is provided to accept the Prime Power to the LGM. The input power will be 115 VAC $\pm$ 10% to 400 Hz. The power cable must have an overall cable shield.

3.3 DETAIL ELECTRICAL DESIGN

3.3.1 Introduction

Common logic elements were designed into P. C. B.'s which were used in more than one unit. This was possible since there are many functions which are similar in these units. Consequently, it was decided to design these cards with emphasis on commonality. Variations in specific unit functions were taken care of by either toggle switches mounted on the P. C. B. or by back-plane wiring. For purposes of this technical report, we will describe the card in detail only once in the first section covering that material; variations of how it will be used in each unit will be covered under that unit.

3.3.2 MUX/DEMUX

3.3.2.1 Common Design

A common P. C. B. is used to perform the multiplexing and demultiplexing function in the LGM, RLGM, and RMC. Evaluations of the variations required by each unit as well as the multiple variations within each unit indicated that a common P. C. B. could be implemented.

The design of the MUX/DEMUX P. C. B. was implemented without the use of ROM's or PROM's. Consequently, the design was implemented using a logic topology which can produce all of the MUX/DEMUX variations by simple toggle switch selection.

3.3.2.2 MUX/DEMUX Requirements

Before a discussion on the operation of the MUX/DEMUX P. C. B. certain system requirements, in terms of the MUX/DEMUX function will be explained.

An examination of the MUX/DEMUX Pattern sequences for the RLGM LGM and RMC reveal that there are only four possible combinations, that is, the sequence of multiplexing or demultiplexing local channels and/or another group input, as in the case of RMC, must be one of four patterns as shown in Figure 3-2. Keep in mind that we are speaking of pattern sequences only, regardless of the number of channels within the group. N in Figure 3-2 could be any number, what is important is the sequence. Associating each MUX/DEMUX pattern sequence (Figure 3-2) with each unit (LGM, RMC, and RLGM) reveals that each pattern is used in the unit indicated.

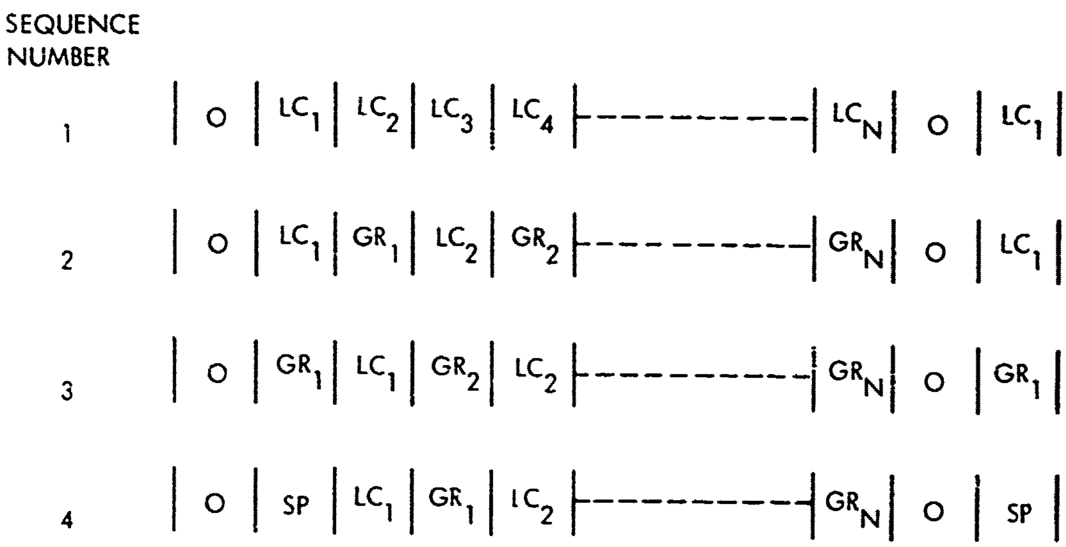
Sequence	Unit		
	RMC	RLGM	LGM
1	X	X	X
2	X		
3	X		
4	X		

As can be seen the RLGM and LGM will always use pattern sequence 1 but the RMC can be operated in any of the four pattern sequences shown.

Now that the pattern sequence has been established, the last piece of information required is the number of channels within the group - the N of Figure 3-2. This is determined by the specification requirement and is summarized in Table 3-3.

TABLE 3-3. NUMBER OF CHANNELS PER GROUP

Sequence	Channels Per Group		
	RMC	RLGM	LGM
1	8 or 9	9	8 or 9 or 16 or 18
2	9 or 16		
3	8		
4	18		



O = OVERHEAD CHANNEL

LC_X = LOCAL CHANNEL

GR_X = GROUP INPUT CHANNEL

SP = SPARE

Figure 3-2. MUX/DEMUX Pattern Sequences

Table 3-3 shows that in the RMC pattern 1 can only be selected for either an 8 or 9 channel group; that the LGM can MUX/DEMUX a pattern 1 sequence for an 8 or 9 or 16 or 18 channel group, and that only the channel groups associated with each pattern sequence need be selected on a per unit basis. There is a maximum of six MUX/DEMUX combinations involved. For example, the RMC can be operated in one of four patterns with one of four channel-per-group combinations. The LGM has only four combinations, the number of channels per group. The RLGM is fixed with pattern 1 and nine channels per group.

As an example of how this would work in an RMC let us look at the multiplexer circuit shown in Figure 3-3. If the local channels are always connected to MUX A and the group input channels are always connected to MUX B the connections to the multiplexer will be as shown in column A, which is all of the combinations for the RMC, that is up to eight local channels multiplexed with eight channels of an incoming group. To multiplex these inputs the pattern and the number of channels in the group must be known. This information will be supplied to the MUX DEMUX card by three toggle switches located on the Timing Generator. Only three switches are required since there are only six combinations as was previously explained. Let us assume that pattern 3 is selected. This means that the pattern sequence for multiplexing is as shown in Figure 3-2 and repeated here.

|←———— 8 Channel Group ————→|

| O | GR1 | LC1 | GR2 | LC2 | GR3 | LC3 | GR4 | O | GR1 | ----

O = Overhead

GR1 = Group Input$_x$

LC1 = Local Input$_x$

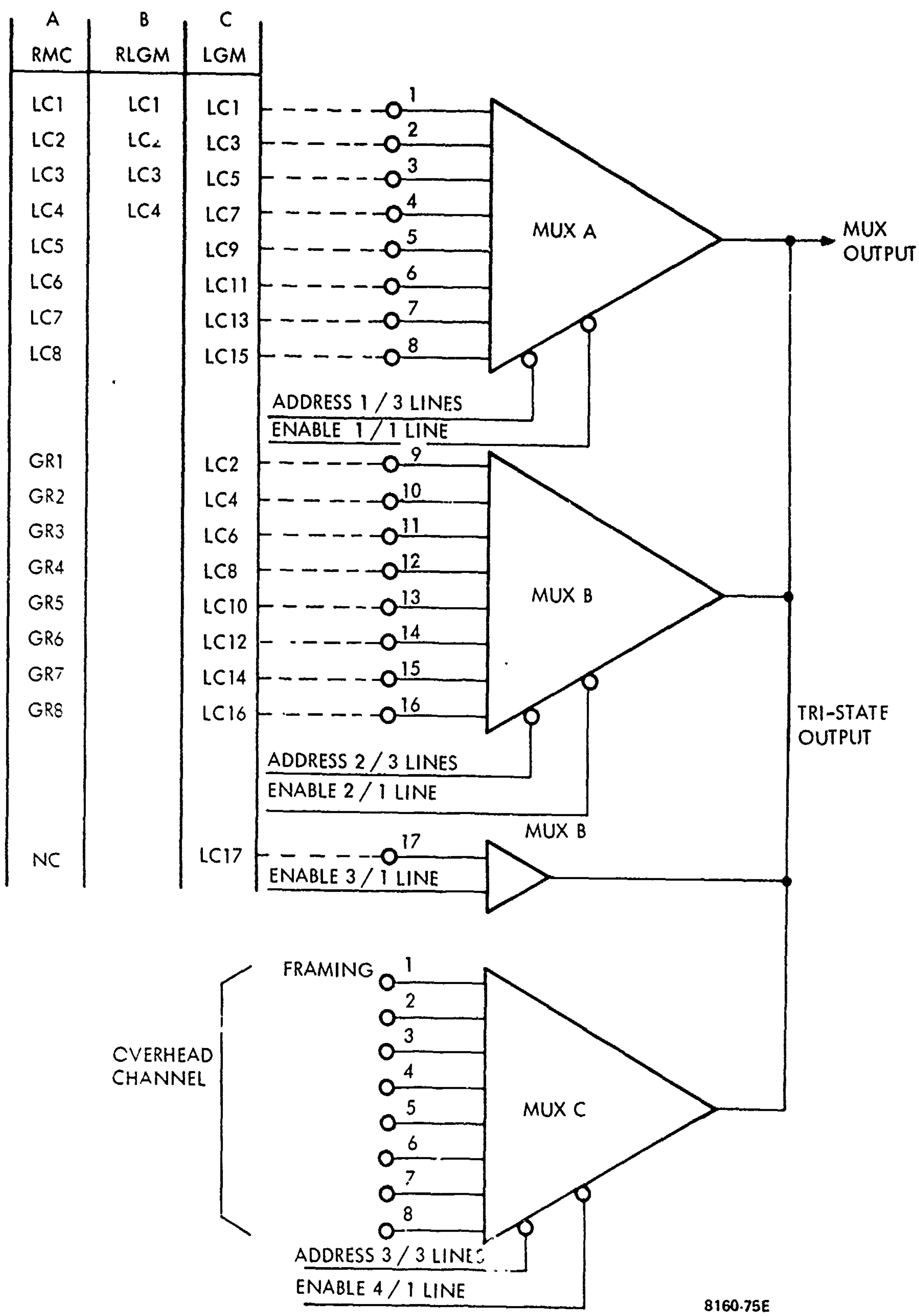


Figure 3-3. MUX Connections for Each Unit

Since pattern 3 in the RMC must be an eight channel group (refer to Table 3-3), and the pattern sequence starts with the first GROUP INPUT channel, only three local phones will be connected. These inputs will be connected to MUX A, inputs 1 through 3 of Figure 3 3.

The MUX/DEMUX logic will cause the address 1, 2, and 3 counters of Figure 3-3 to clear such that each address line is zero. When each MUX is enabled line 1 of MUX A, line 9 of MUX B or line 1 of MUX C will be selected.

The following multiplexer sequence will then be followed:

- ENABLE 4 line will become active gating the framing sub-channel into the MUX OUTPUT line.
- At the next group clock - ENABLE 2 will be active, ENABLE 3 will be inactive and the address 3 counter will advance by one.
- With ENABLE 2 active, line nine (9) will be enabled gating the group input line 1 into the MUX OUTPUT line.
- At the next group clock - ENABLE 1 will become active, ENABLE 2 will be inactive and the address 2 counter will advance by one.
- With ENABLE 1 active, line one (1) will be enabled gating the local channel 1 line into the MUX OUTPUT line.
- At the next group clock ENABLE 2 will be come active, ENABLE 1 will be inactive and the address 1 counter will advance by one.
- With ENABLE 2 active, line ten (10) will be enabled gating the group input line 2 into the MUX OUTPUT line.
- This sequence continues for eight group clock pulses, whereupon the address 1 and address 2 counters are cleared and the ENABLE 4 line becomes active gating the second overhead sub-channel into the bus.
- At the next group clock ENABLE 2 line becomes active and the sequence just described is repeated.

If pattern 2 were to be selected by the toggle switches, the sequence just described would repeat except that the ENABLE 1 line would be active before ENABLE 2. This would multiplex the output with local channel 1 in the first channel following the overhead and the first group input line in the third channel slot.

3.3.2.3 MUX/DEMUX Variations for RLGM and LGM

The above discussions demonstrated how the MUX/DEMUX function would operate in the RMC. Operation of the card in the RLGM is modified, since the RLG output pattern sequence is fixed. Column B of Figure 3-3 shows how the RLGM connections are made. The most significant bit of the address lines to MUX A is grounded in the backplane wiring. The overhead channel is gated onto the output bus followed by inputs 1 through 4 scanned twice. The result is a 4-1/2 channel group which will be:

0 | LC1 | LC2 | LC3 | LC4 | LC1 | LC2 | LC3 | LC4 | 0 | LC1 | ---

This, MUX A is scanned in the RLGM using the same control logic of sequence 1 (nine channels) in the RMC. Because of the wiring variation in the backplane and the assignment of local channels, the same card may be used in the RLGM.

Column C of Figure 3-3 shows the connections for an LGM. As may be seen from Figure 3-3, the local channels are assigned alternately to MUX A and MUX B. The pattern sequence logic used to generate the group output is sequence 2 but, because of the assignment of alternating channels, the pattern generated is sequence number 1. When an 18 channel output is desired from the LGM, the logic for sequence 4 is employed to generate an output with a spare channel in the first position after the overhead channel. The appearance of an 18 channel output from an LGM would be:

0 | SP | LC1 | LC2 | LC3 | --- | LC16 | 0 | SP

Again, due to the alternate assignments of channels to MUX A and MUX B, the proper sequence of output channels is generated.

3.3.2.4 MUX/DEMUX Card

A block diagram of the MUX/DEMUX P.C.B. is shown in Figure 3-4.

Programming is accomplished by the use of three switches located on the edge of the Timing Generator. The switch outputs are encoded on the Timing Generator and transferred to the MUX/DEMUX card to control the output

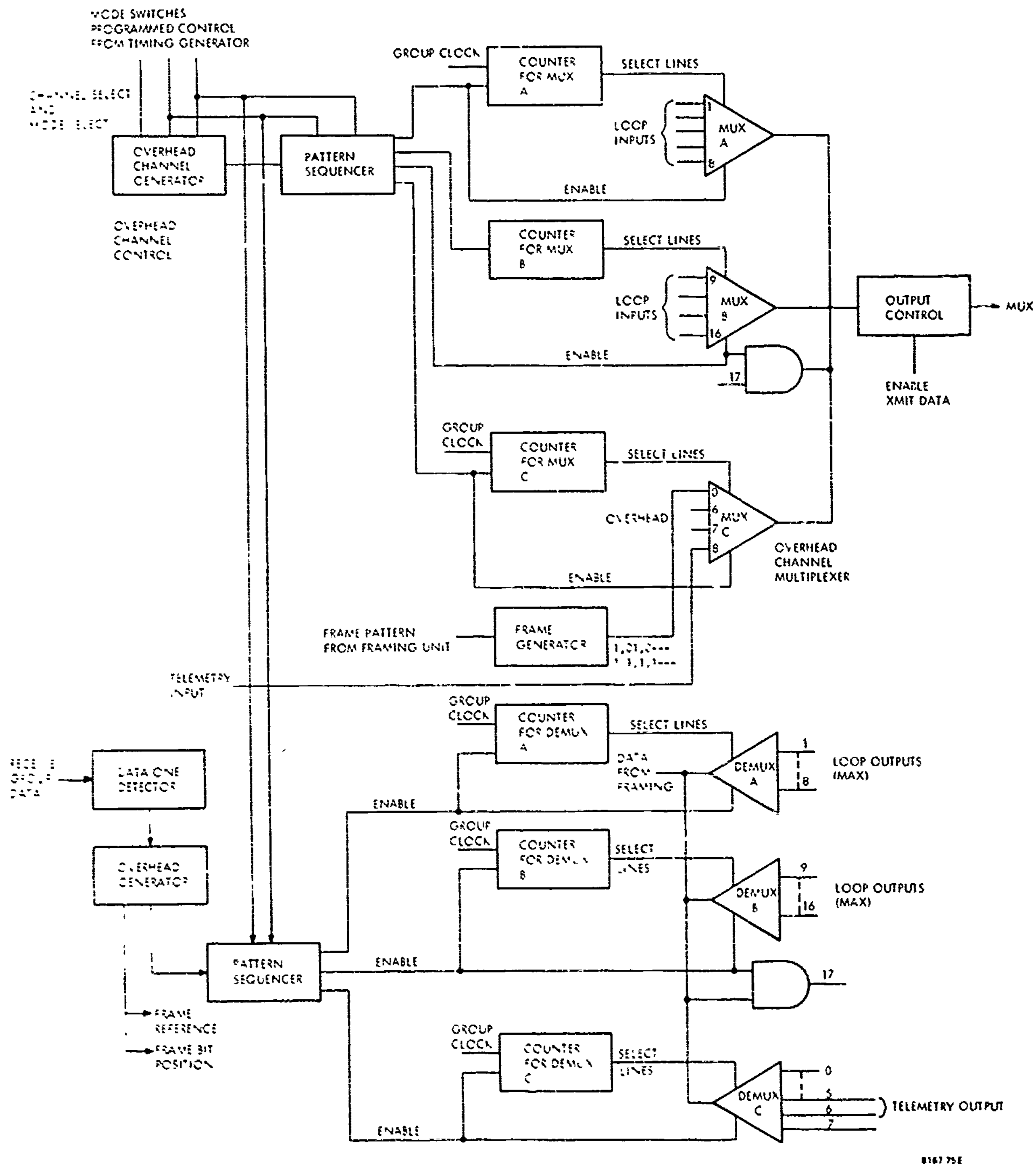


Figure 3-4. MUX DEMUX Block Diagram

Pattern Sequencer. In addition, a counter (Overhead Channel Generator) is preset to the proper value to divide the group rate clock (controlled by the same switches) by 8, 9, 16 or 18. This establishes where in the pattern of the group output to insert the data from the overhead channel and data from the Loop modems.

The multiplexer function contains three 8 bit multiplexers (A, B and C) and one additional input for the 17 Loop inputs and 8 overhead sub-channels. The Pattern Sequence provides the enable inputs to the multiplexers and produces one of the pre-selected output patterns of Figure 3-5, LGM Output Group Patterns.

Multiplexer C. is dedicated to the 8 sub-channels that together make up the overhead channel. (See Figure 3-5 Overhead channel.) The first of these sub-channels contains the Frame information from the Frame Generator, and will be alternating 1 - 0 or all 1's as selected by the Frame Pattern signal from the Group Framing card. Channel 8 of the sub-channels (subchannel before the framing subchannel) is for local telemetry. The remaining subchannels are set to logic level "1."

The output control circuitry inhibits the data channels from the MUX output upon command from the Group Framing card. The Enable Xmit Data signal causes the output of either normal data or all 0's. In either case, the frame pattern is passed through unaltered by the Output Control Logic.

The programmable DEMUX receives reframed data and a frame reference from the framing card and demultiplexes the data into loop channels and overhead subchannels in a preselected manner similar to the multiplexer. The eighth subchannel (subchannel just before the framing subchannel) containing SYSCON Telemetry is demultiplexed and routed to a card output.

NO. OF CHAN.	NO. OF LOOPS	PATTERN
8	7	O L1 L2 L3 L4 L5 L6 L7 O L1 L2 L3 . . . .
9	8	O L1 L2 L3 L4 L5 L6 L7 L8 O L1 L2 L3 . . . .
16	15	O L1 L2 L3 L4 L5 L6 L7 L8 L9 L10 L11 L12 L13 L14 L15 O L1 L2 L3 . . . .
18	16	O SP L1 L2 L3 L4 L5 L6 L7 L8 L9 L10 L11 L12 L13 L14 L15 L16 O SP L1 L2 L3 . . . .

OVERHEAD CHANNEL

	F	1	2	3	4	5	6	T	F	1
TO/FROM SUB CH.	1	2	3	4	5	6	7	8	1	2

F = FRAME BIT FROM FRAME SUBCHANNEL

{. 1,1,1 . . . OR . 1,0,1,0, . . .}

8133-75E

Figure 3-5. LGM Output Group Patterns and Overhead Channels

3.3.3 Group Framing Unit

The original framing procedure was to occupy two printed circuit cards the framing card and the synchronizer card. Because of design simplification, both these functions eventually required only one printed circuit card referred to as the Group Framing card.

The framing portion of the card consists mainly of counters that monitor the incoming data and count errors in the framing patterns to determine frame status. The primary outputs from the framing portion of the card are "received side in/out of frame" and "remote side in/out frame."

The function of the synchronizer portion of the card is to interpret the frame status information and control the received data, the transmit data, frame output pattern and resync information to the TED.

3.3.3.1 Framing

The group framing unit is used in the receive side of all group data streams and controls the acquisition and maintenance of frame synchronization and generates frame error counts. The frame generator, in the block diagram of Figure 3-6 aligns itself with the framing pattern contained within the overhead channel of the data stream.

During the framing process, all the data transmitted by the remote unit has been set to zero with the exception of the first subchannel of the overhead channel (location of the framing sub-channel). Figure 3-7 illustrates the group and overhead channel formats. This channel contains a framing pattern of all "1's" or alternate "1's" and "0's." The framing unit interface is shown in Table 3-4.

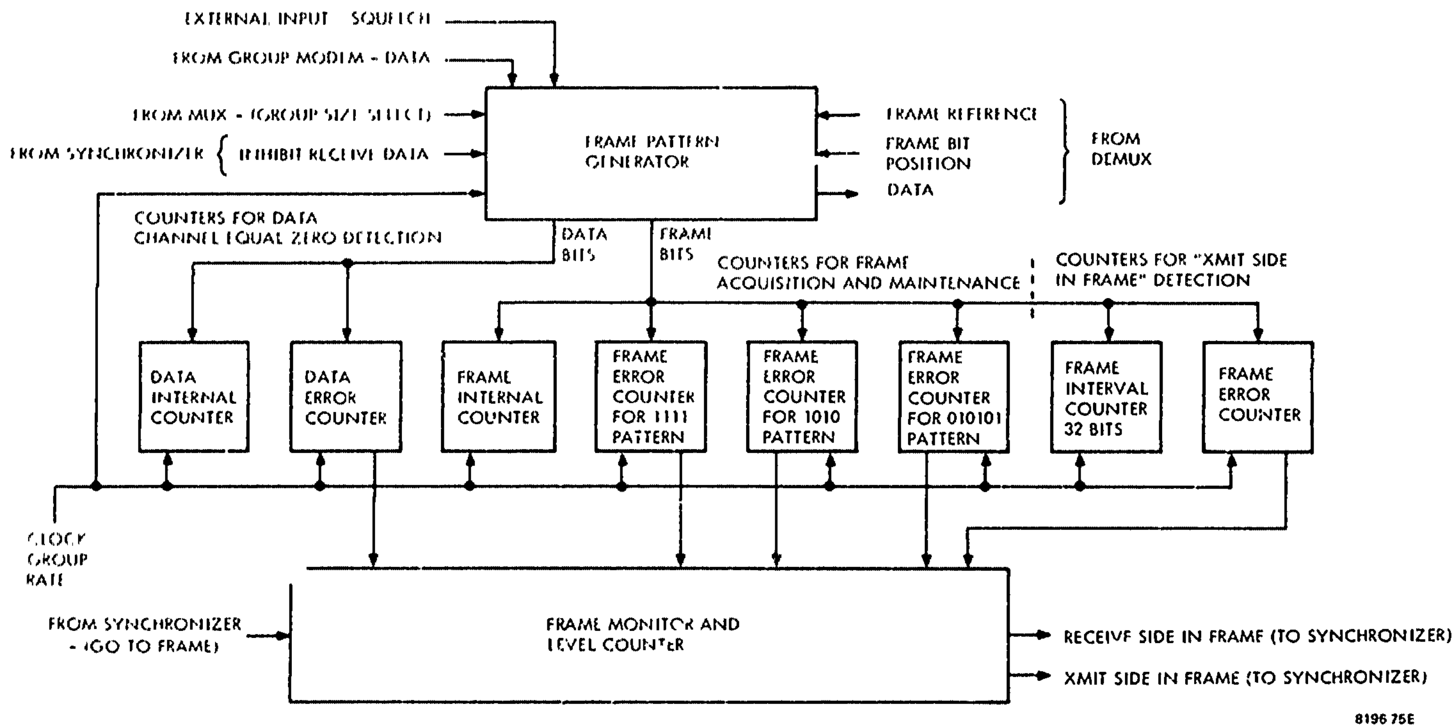


Figure 3-6. Framing Block Diagram

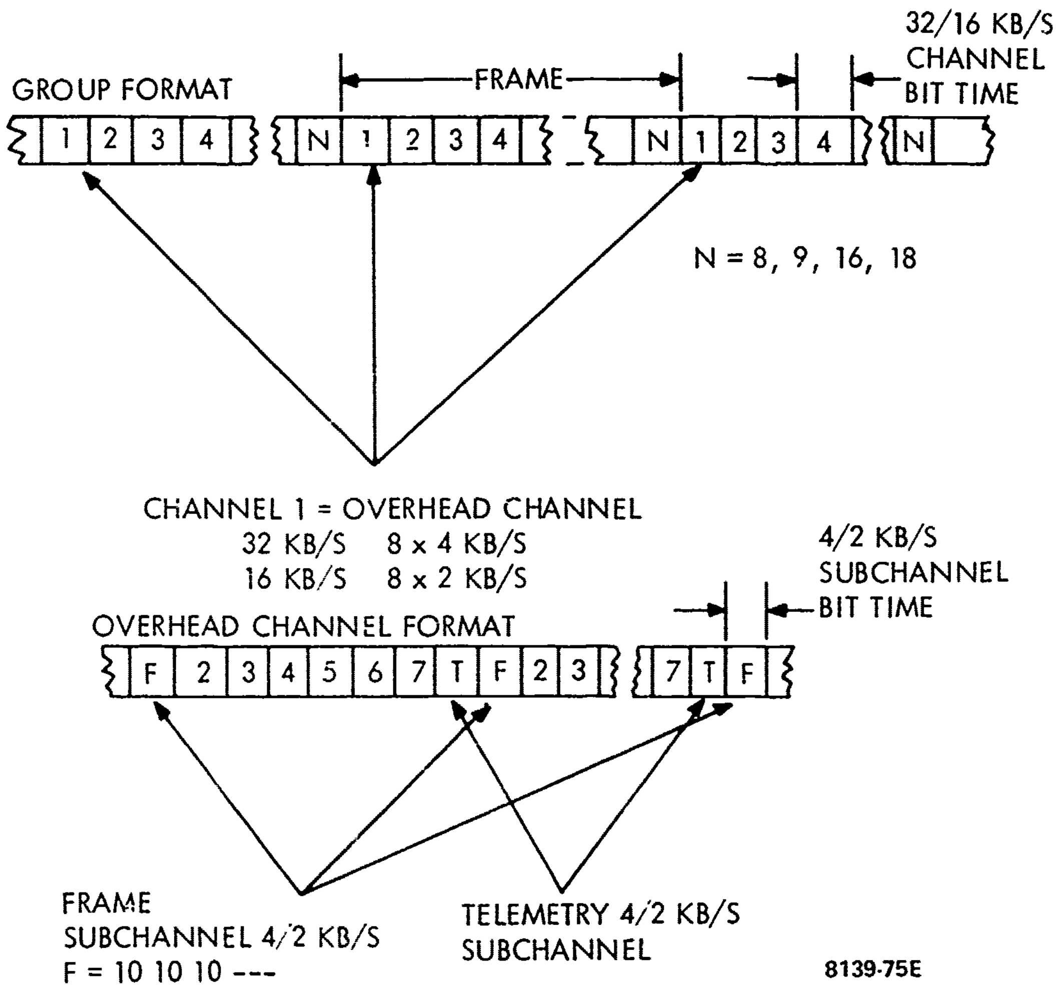


Figure 3-7. LGM Group and Overhead Channel Formats

TABLE 3-4. FRAMING UNIT INTERFACE

Inputs:		
1.	"Go to Frame"	Command from the synchronizer logic 0 pulse of a period of 1/group rate.
2.	Inhibit Receive Data	Level from the synchronizer 0 = sets downstream data to one's 1 = enables downstream data
3.	Group Size Select	4 line input for 4, 5, 9, 16 or 18 channels, level "1" on any one line select group size. All lines logic 0 for 8 channels.
4.	Data	Baseband data from demodulator, levels compatible with CMOS circuitry.
5.	Clock	At group bit rate, 50% duty cycle.
6.	Squelch	Input level 0 = inhibit frame search 1 = enable frame search
7.	Frame Reference	Logic "1" pulse of width 1/group rate at a frequency of 4 kHz, in phase with internally generated frame pattern.
Outputs:		
1.	Data	Baseband data out
2.	Error Out	Single output line, level is active high indicating an error in the frame pattern
3.	Receive Side in Frame	Level to synchronizer "1" = in frame "0" = out of frame
4.	Xmit Side in Frame	Level to synchronizer "1" = in frame "0" = out of frame

Note: All levels compatible with CMOS Logic.

Upon a command of the synchronizer to "go to frame" the framing unit sends a command to the demultiplexer to search for a data "one". When the demultiplexer detects a "one" it begins generating a frame reference signal, a 2K/1k Hz square wave aligned with the "1-0-1-0" pattern, and a "frame bit" pulse indicating the position of the first subchannel. The framing unit uses this information to generate an internal "1-1-1-1", "0-1-0-1" and "1-0-1-0" framing patterns. At the proper bit intervals, the interval framing patterns are compared to the received data and, if different, error pulses are generated and counted over predetermined intervals.

Because the framing unit does not know which pattern is being received, errors for both the all 1's pattern and the alternate "1 - 0" pattern must be counted, and in addition, because there might be a phase error in the received "1 - 0" pattern and the internally generated "1 - 0" pattern errors must be counted for an alternating "0 - 1" pattern. This phase error can occur when the generator, which is a counter that locates the position of the framing bit, locks onto an all "1's" pattern and then the pattern is switched to an alternating pattern

Frame acquisition is a three level process controlled by the frame monitor, in which, during each level, the outputs of the counters are examined at the completion of a predetermined interval and, if the number of errors are below thresholds, the acquisition level is advanced. The acquisition process is shown in flow chart form in Figure 3-8 and the criteria that must be met to advance from one level to the next is diagrammed in Figure 3-9.

The frame monitor begins the four level process upon a "go to frame" command from the synchronizer; level 1 is achieved upon the detection of the first data "one". In level 1, the 3rd framing bit is examined and must be a data "1" to advance to level 2 where two of the three bits 5, 6, and 9 must be data "1's". In level 3, frame bits 10 through 41 are examined. If 30 of the 32 bits are correct for the 0101 pattern, the 1010 pattern or the 1111 pattern, with an indication of zero data on the channels, "in frame" is declared and the system advanced to maintenance mode (level four).

If, at any time, in levels one, two, or three, the criteria cannot be met, a search command is initiated and the system awaits another data "1", restarting the acquisition process.

The detection of the condition that data in the channels is equal to logic 0's is accomplished by 2 counters. One counts the position of data bits and one counts the data "1's" in these positions. If there are fewer than 171 data "1's" out of a 512 bit sample, a level is set indicating that data in the channels is equal to zero. The detection circuit runs continuously and is independent of the circuits used for acquisition and maintenance. A flow chart of this detection sequence is shown in Figure 3-10.

In the maintenance mode (level four) the frame bits are examined over 100 bit intervals; errors are counted for the 010101, 101010, and 1111 pattern and if 58 of these 100 bits are correct for the 010101 or 101010 patterns or for the 1111 pattern with an indication of zero data on the channels, an indication of "inframe" is maintained.

If, at any time, the criteria cannot be met, the next 100 bits are examined and if the test fails a second time "out of frame" is indicated to the synchronizer. The system continues to test 100 bit samples.

Another detection circuit that runs independent of the acquisition and maintenance circuitry monitors the frame bits over 32 bit intervals to determine which framing pattern is being received. Once 30 out of 32 frame bits are correct for the 1010 frame pattern or the 0101 pattern, a level is set indicating that the "transmit side is in frame sync." The 1111 frame pattern is then monitored and when 30 out of 32 frame bits are correct for this pattern and there is an indication of zero data on the channels, a level is set indicating that the "transmit side is not in frame sync." The flow chart of this sequence is shown in Figure 3-11.

The "squelch" input to framing unit is a DC level from an external input. A logic 0 forces an inframe condition on the receive side and enables data and the 1010 frame pattern to be transmitted. Refer to Table 3-4.

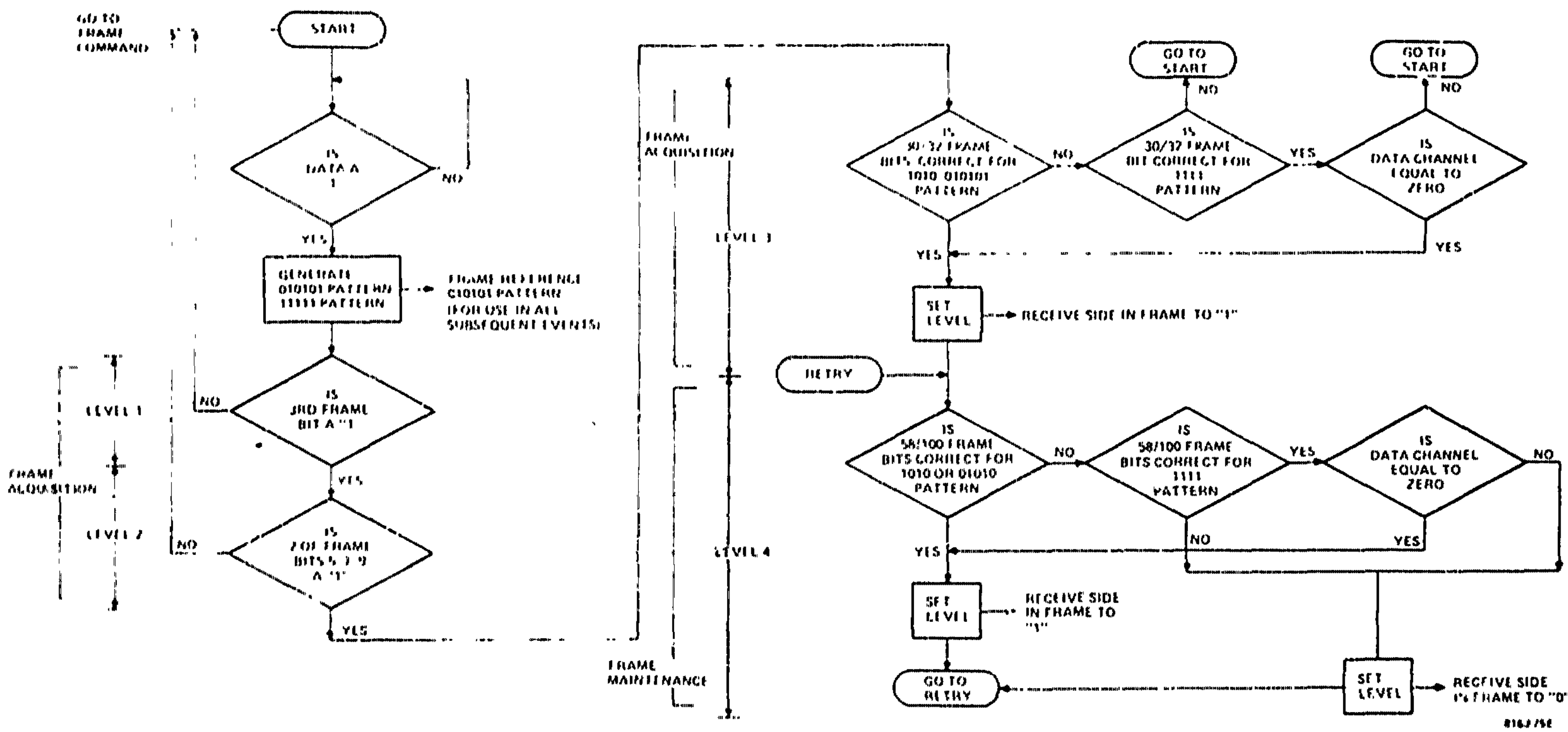


Figure 3-8. Frame Acquisition and Maintenance Flow Chart

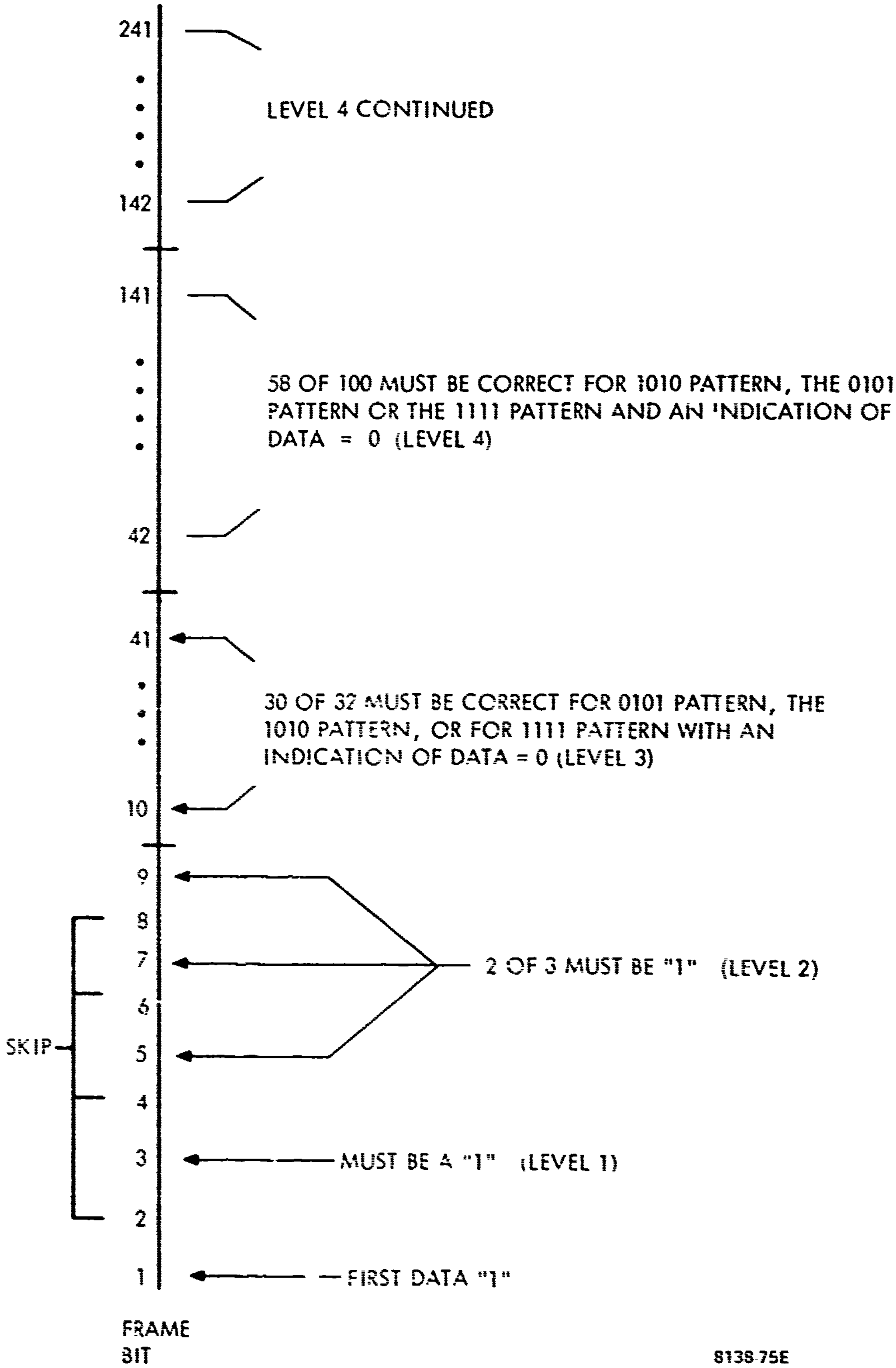
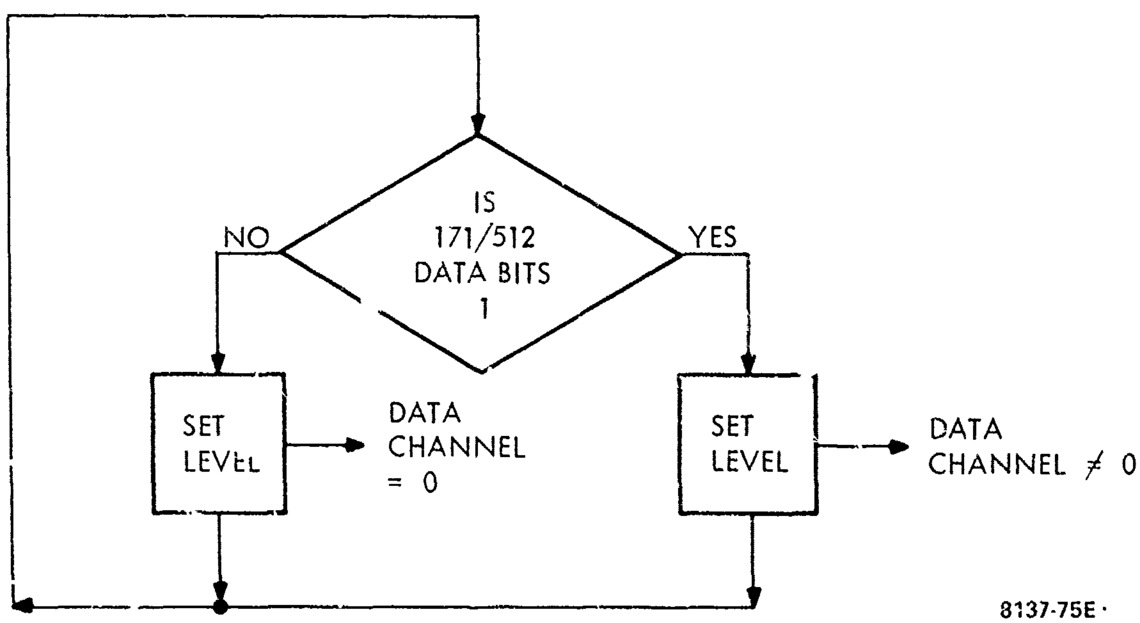


Figure 3-9. Framing Sequence



F··ure 3-10. "Data Channel Equal To Zero" Detection Flow Chart

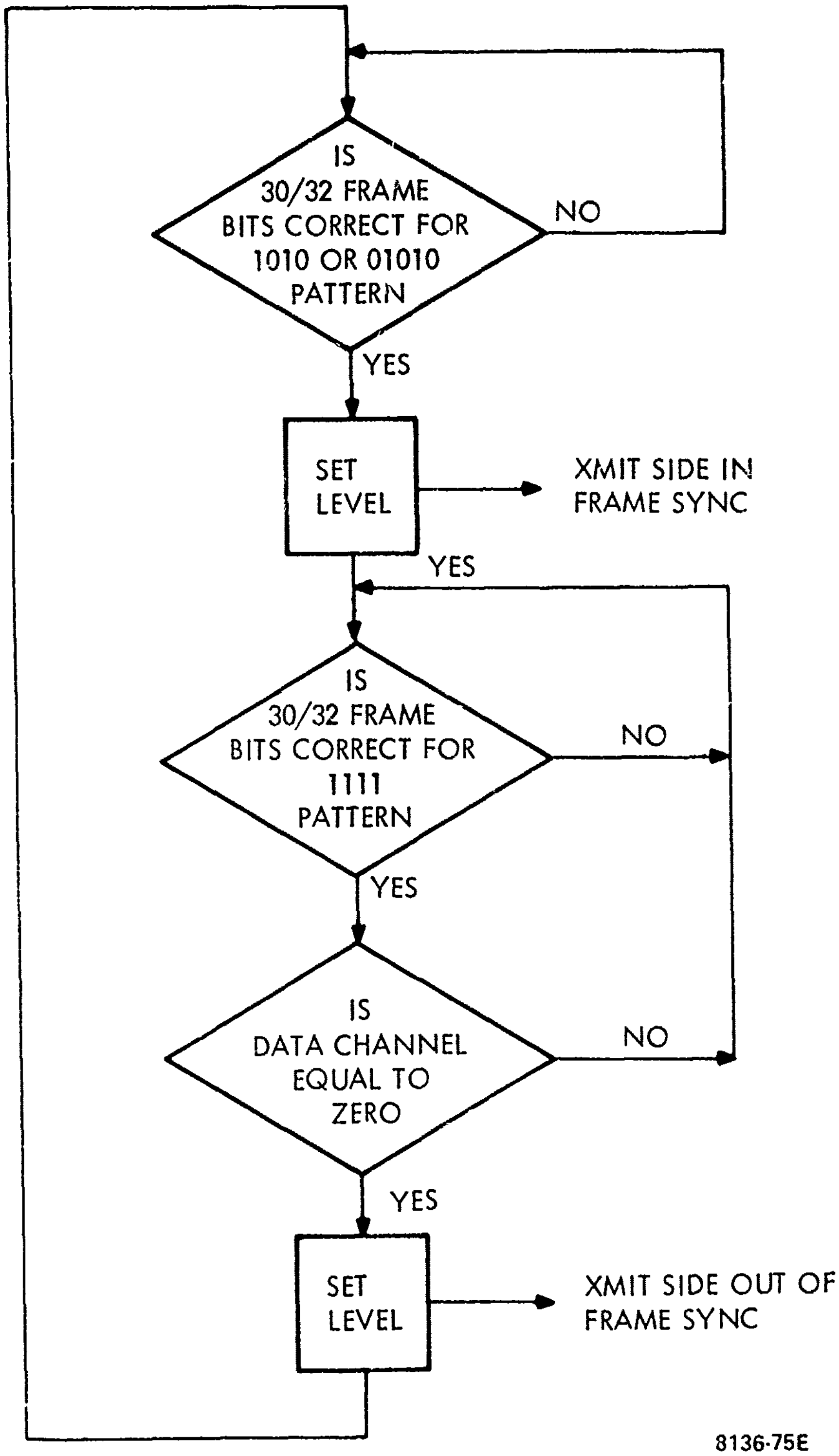


Figure 3-11. "Xmit Side in Frame" Detection Flow Chart

The "Inhibit Receive Data" input from the synchronizer controls the received data. A logic 0 sets all received data to "1's." Refer to Table 3-4.

3.3.3.2 Synchronizer

Control of the sequence of operations necessary to obtain link synchronization is the main task of the synchronizer unit, shown in the block diagram of Figure 3-12. The setps in the logic sequence are shown in the flow chart of Figure 3-13. In that figure, signals from the framing unit are monitored for change of state; when the framing unit declares the receive group signal "Out of Frame", the chain of events down the right side of the chart occurs.

After a 0.5 second delay (which may be switched out) traffic flowing to downstream loops is set to all "1's", the frame pattern set to all "1's", and the transmitted data set to all "0's." Next, a timeout of 2.13 seconds is started and the TED checked for sync in progress; if sync is not in progress, a command is sent to the TED to begin synchronization. After a 500 μsecond delay, in-sync status is checked and, when received, a "go to frame command" is sent to the framing unit commanding it to search for frame. In-frame status is awaited and when received, the transmitted framing pattern is changed to alternate "1's" and "0's" and the downstream data enabled. The received frame pattern is checked: if the pattern indicates the transmit side is in frame-sync the transmitted data is enabled and the sequence returned to the starting point. If frame sync cannot be achieved within approximately 2.13 seconds, the sequence is returned to the entry point labeled RETRY on the flow chart. If frame cannot be achieved, an alarm is set and not cleared until the receive side is declared in-frame sync.

If the framing unit detects a frame pattern change to all "1's", but the received side is still in sync, the sequence down the left side of the flow chart is followed. The transmit data, except for the framing sub-channel, is set to all "0's" until 1010 framing pattern is received. Failure to receive in-sync status within approximately 14 seconds causes the circuit to try again until the 1010 framing pattern is received. Frame status and frame alarm are supplied to the

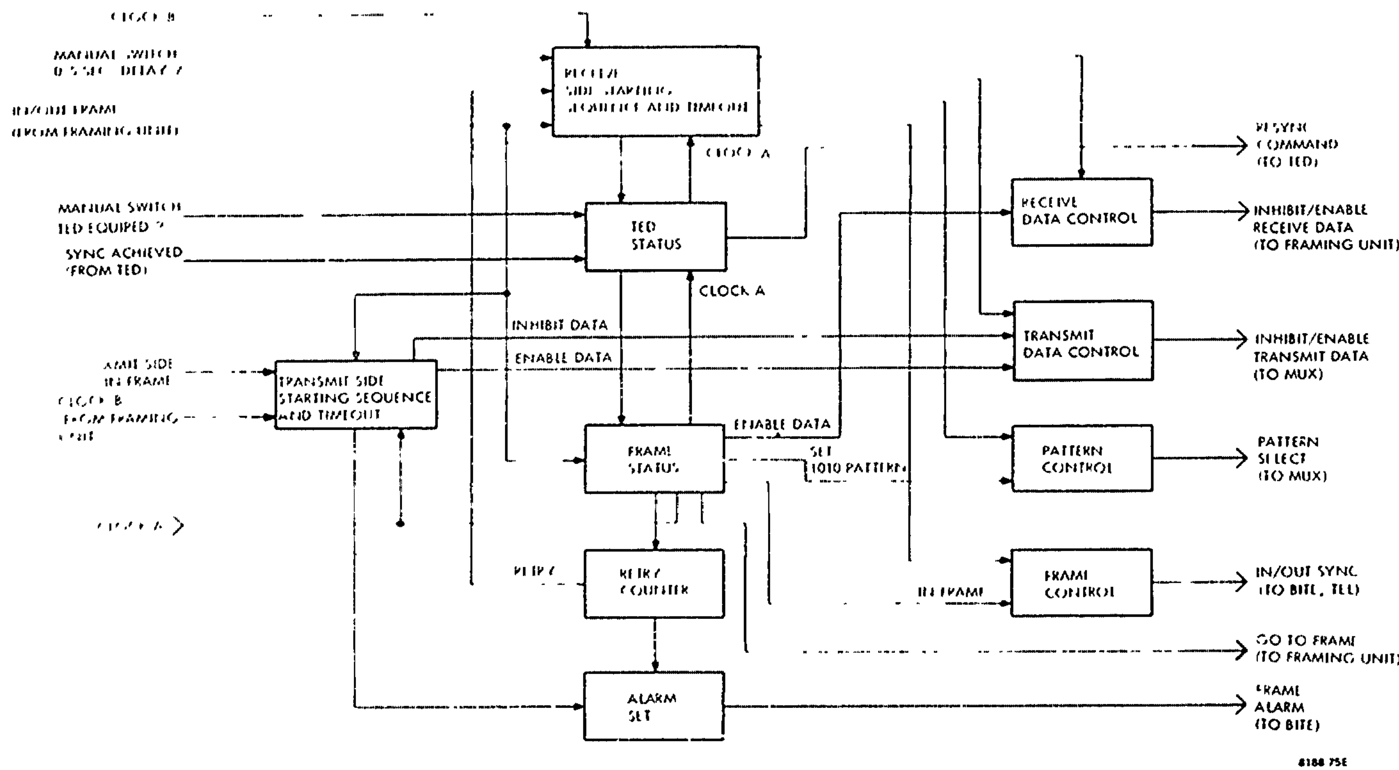


Figure 3-12. Frame Synchronizer Block Diagram

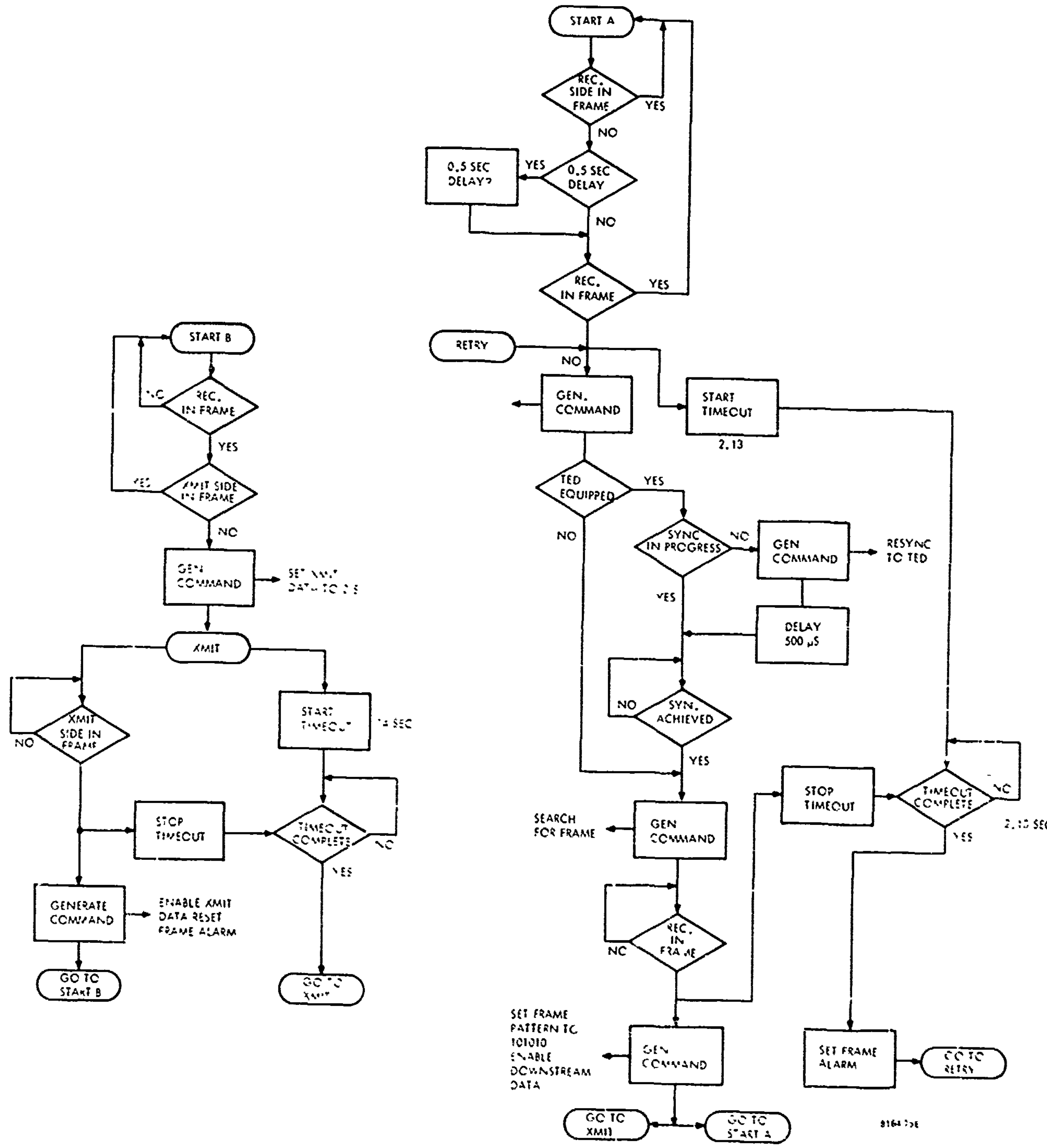


Figure 3-13. Synchronizer Flow Chart

BITE card. Three LED's are supplied on the Group Framing card and their functions are as follows:

a. BITE indicator

b. Frame Alarm

c. TED alarm - illuminated when the TED is not in synchronism

Table 3-5 is a list of the interface levels to the synchronizer.

3.3.4 Timing Generator/Telemetry - LGM

The same Timing Generator is used in the RMC, RLGM and LGM. Various combinations of rates are used in the units; the rate combinations required in the LGM are generated by the circuitry shown in block diagram form in Figure 3-14. Table 3-6 shows the clock rate required, the rate switch codes, and the configurations where the rates are required.

In the LGM, the Timing Generator is locked to either the Station Clock input or the clock associated with the NRZ Group Data input; they are both the same frequency and differ only in phase.

Line drivers and receivers for SYSCON Telemetry access are placed on the Timing Generator, as is the switch to route Telemetry loop-back internally or externally, the relay for the SA Alarm and the gate which breaks the Telemetry loop if the BITE indicates a fault. Interface drivers and receivers for the TED and Frame Squelch inputs (used only in the LGM) and the receiver for the Station Clock input are also placed on the Timing Generator card. Details of the circuit implementation for the interface drivers and receivers are given in Section 3.3.6. Details of the Timing Generator implementation are covered in Section 7.3.6.

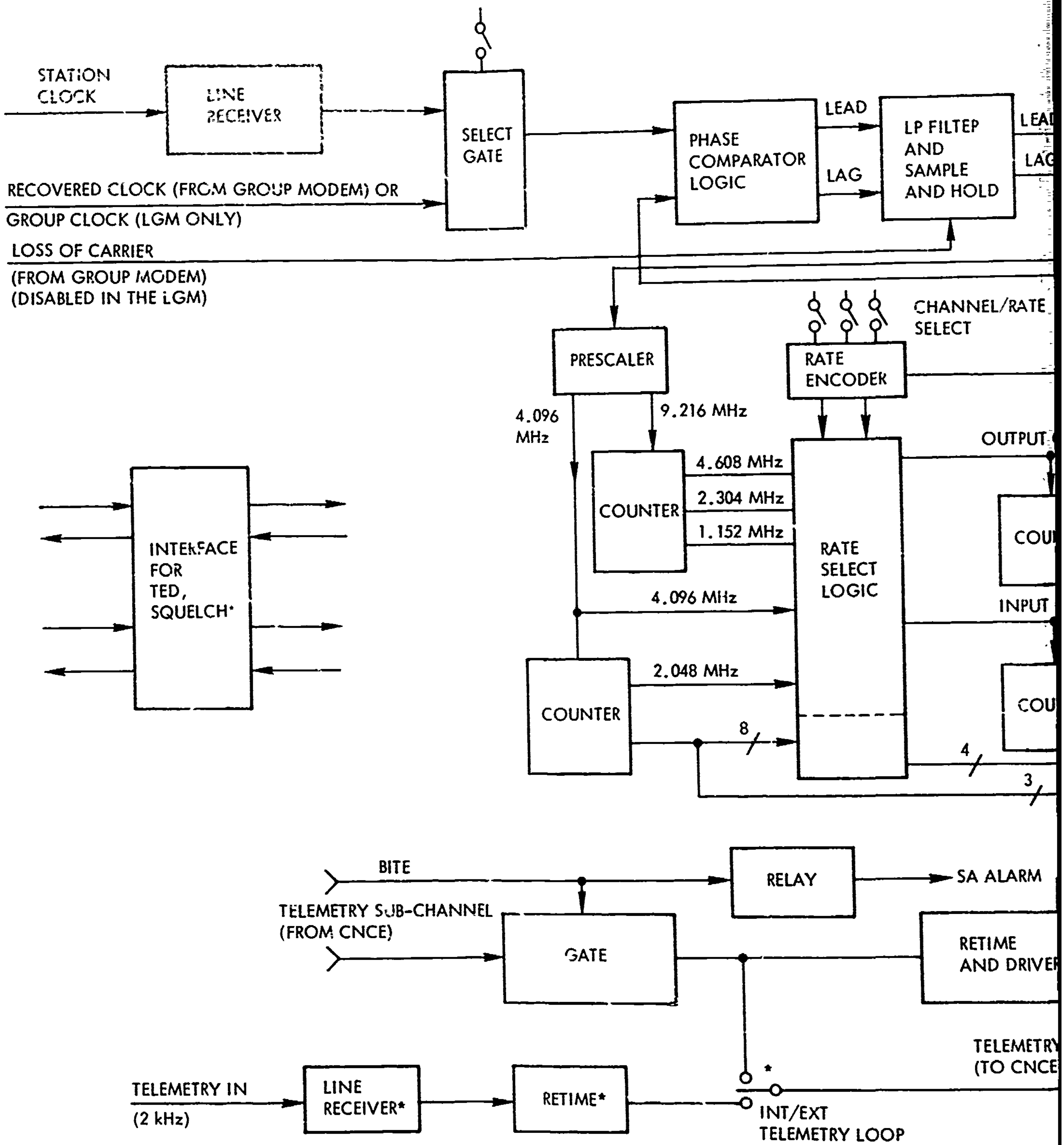
3.3.5 Loop Modem

The Loop Modem is a WF-16 field wire carrier terminal which provides full duplex transmission of binary data signals at 32, 16 kb/s between DSVT terminals and the LGM. A phantom power loop is provided in the diphase output

TABLE 3-5. INTERFACE LEVELS TO SYNCHRONIZER

Input:	
Xmit side in frame	Level from framing unit 0 = receiving 1111 pattern 1 = receiving 1010 pattern
Receive side in frame	Level from framing unit 0 = out of frame 1 = in frame
Sync achieved	Level from TED, balanced signal 0 = sync in progress 1 = sync achieved
0.5 sec delay	Level set by manual switch 0 = No delay (switch closed) 1 = Delay enabled (switch open)
TED Equipped	Level set by manual switch 0 = TED Equipped (switch closed) 1 = Not TED Equipped (switch open)
Clock A	32 kHz, 50% duty cycle
Clock B	150 Hz, 10 - 90% duty cycle
Output:	
Inhibit/enable receive data	Output level to framing unit 0 = inhibit receive data 1 = enable receive data
Inhibit/enable transmit data	Output level to multiplexer 0 = inhibit data 1 = enable data
Pattern select	Output level to multiplexer 0 = 1111 pattern 1 = 1010 pattern
In/out frame sync	Output level to BITE 0 = out of sync 1 = in sync
Frame alarm	Output level to BITE 0 = frame alarm 1 = no alarm
Resync command	Balanced output to TED 32 μs positive pulse
Go to frame	Command to framing unit of period 1/32K

Note: All levels are C-MOS compatible.



STATION CLOCK
LINE RECEIVER
SELECT GATE
RECOVERED CLOCK (FROM GROUP MODEM) OR
GROUP CLOCK (LGM ONLY)
LOSS OF CARRIER
(FROM GROUP MODEM)
(DISABLED IN THE LGM)
PHASE COMPARATOR LOGIC
LEAD
LAG
LP FILTER AND SAMPLE AND HOLD
CHANNEL/RATE SELECT
PRESCALER
RATE ENCODER
4.096 MHz
9.216 MHz
COUNTER
4.608 MHz
2.304 MHz
1.152 MHz
RATE SELECT LOGIC
OUTPUT
INPUT
4.096 MHz
2.048 MHz
COUNTER
8
4
3
INTERFACE FOR TED, SQUELCH*
BITE
RELAY
SA ALARM
TELEMETRY SUB-CHANNEL (FROM CNCE)
GATE
RETIME AND DRIVER
TELEMETRY (TO CNCE)
TELEMETRY IN (2 kHz)
LINE RECEIVER*
RETIME*
INT/EXT TELEMETRY LOOP

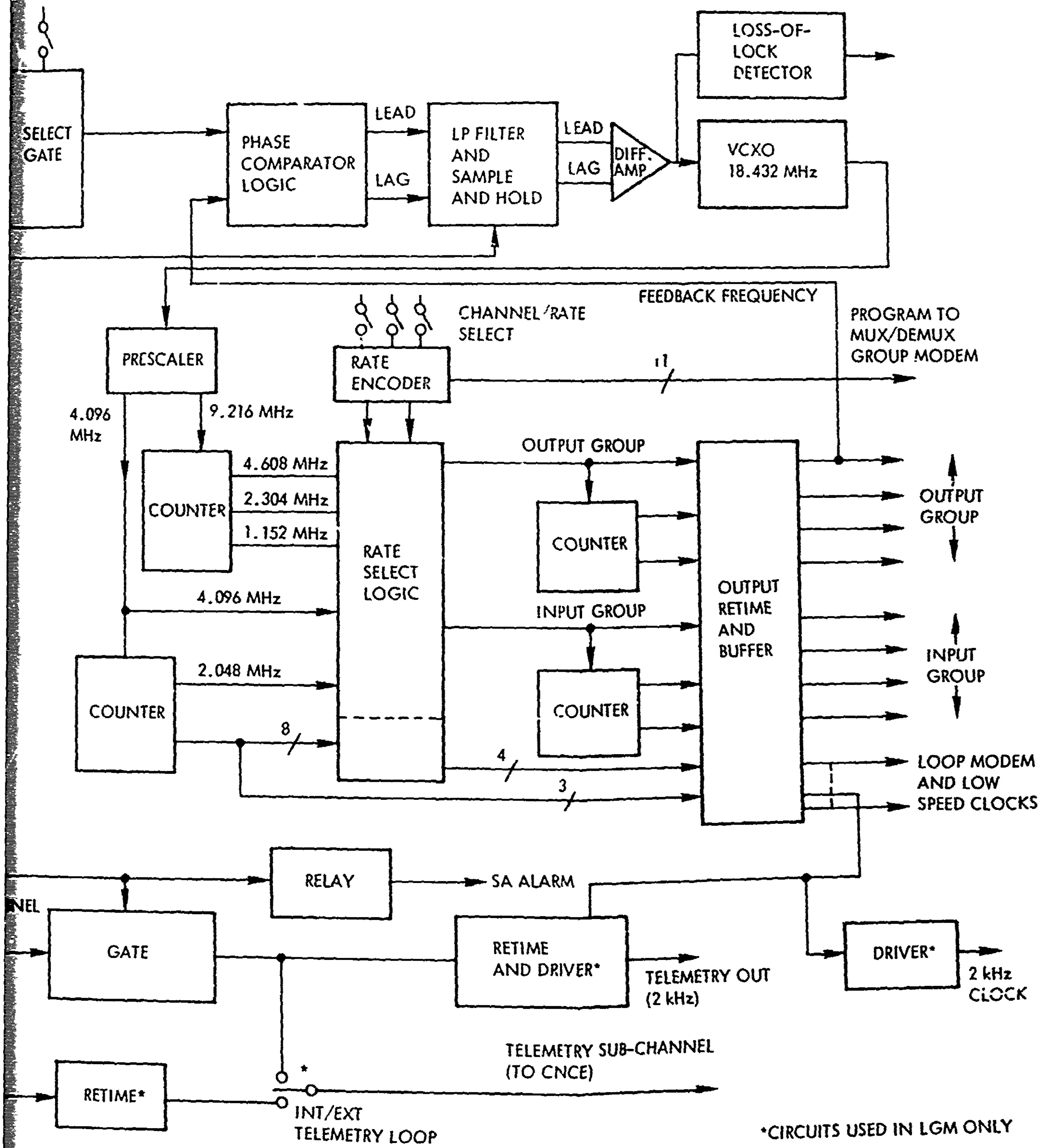


Figure 3-14. LGM Block Diagram

TABLE 3-6. TIMING GENERATOR OUTPUTS

RLGM Configuration	-	4 1/2 Chan	-	-	-	-
LGM Configuration	8 Chan	9 Chan	-	-	16 Chan	18 Chan
RMC Configuration Input	4 1/2 Chan	4 1/2 Chan	-	-	8 Chan	9 Chan
RMC Configuration Output	8 Chan	9 Chan	8 Chan	9 Chan	16 Chan	18 Chan
Switch 1	1	1	0	0	1	1
Switch 2	0	1	0	1	0	1
Switch 3	1	0	1	0	0	1
CLOCKS						
* Station Clock, Recovered Clock, or Data Clock Input	256	288	256	288	512	576
* Output Group	256	288	256	288	512	576
* 2X Output Group	512	576	512	576	1024	1152
* 8X Output Group	2048	2304	2048	2304	4096	4608
* Input Group	144	144	144	144	256	288
* 2X Input Group	288	288	288	288	512	576
* 8X Input Group	1152	1152	1152	1152	2048	2304
* Loop Modem Clock 1	512	512	512	512	512	512
* Loop Modem Clock 2	64	64	64	64	64	64
* Loop Modem Clock 3	32	32	32	32	32	32
Group Framing Clock	32	32	32	32	32	32
Telemetry Clock	2	2	2	2	2	2
Timeout Clock	0.15	0.15	0.15	0.15	0.15	0.15

NOTES: 1. * Rates halve when 16 kb/s DSVT's are used

2. All rates are in KHz

loop to power the DSVT. The phantom loop power feed is illustrated in Figure 3-15. The maximum current drawn by the off-hook DSVT is 83.3 mA with no battery charging current. The corresponding maximum reliable operating range is 3.0 Km (refer to Figure 3-16). The current limiter is set to trip at 250 mA for short circuit protection. The open circuit threshold is set at 3 mA, that is, if the loop current is ever less than 3 mA, the power feed open circuit detector will cause an alarm to be generated. A manual switch provides for disconnecting power from the loop for maintenance purposes. This switch is also be used to disable the summary status alarm signal when a loop modem is not connected to a DSVT.

The current limiter is designed to pass a transient current of up to 180 mA peak for 45 milliseconds without shutdown. The DSVT creates a transient which was discovered during interface testing with the V2-model DSVT.

3.3.5.1 Diphase Modulator

Figure 3-17 is a block diagram of the Diphase Modulator. The line receiver converts the balanced NRZ baseband to CMOS logic levels. Figure 3-18 shows how diphase data is generated. When the data is a mark (one) the J-K flip-flop toggles. The output of the J-K flip-flop is conditioned baseband. A transition in the conditioned baseband represents a mark (one).

The conditioned baseband is modulo two added to the bit rate clock (square wave). The resulting output is a conditioned diphase modulated version of the input baseband data. The diphase is retimed by the D flip-flop to remove glitches. The data activity detector generates a control signal indicating the presence of data activity at the baseband input. The modulator output is controlled by the baseband data activity line and the carrier presence detector line. If these signals indicate input data activity and/or carrier presence for a period of approximately 50 ms, the modulator output is enabled. The low-pass filter attenuates diphase signal out-of-band frequency components which might generate

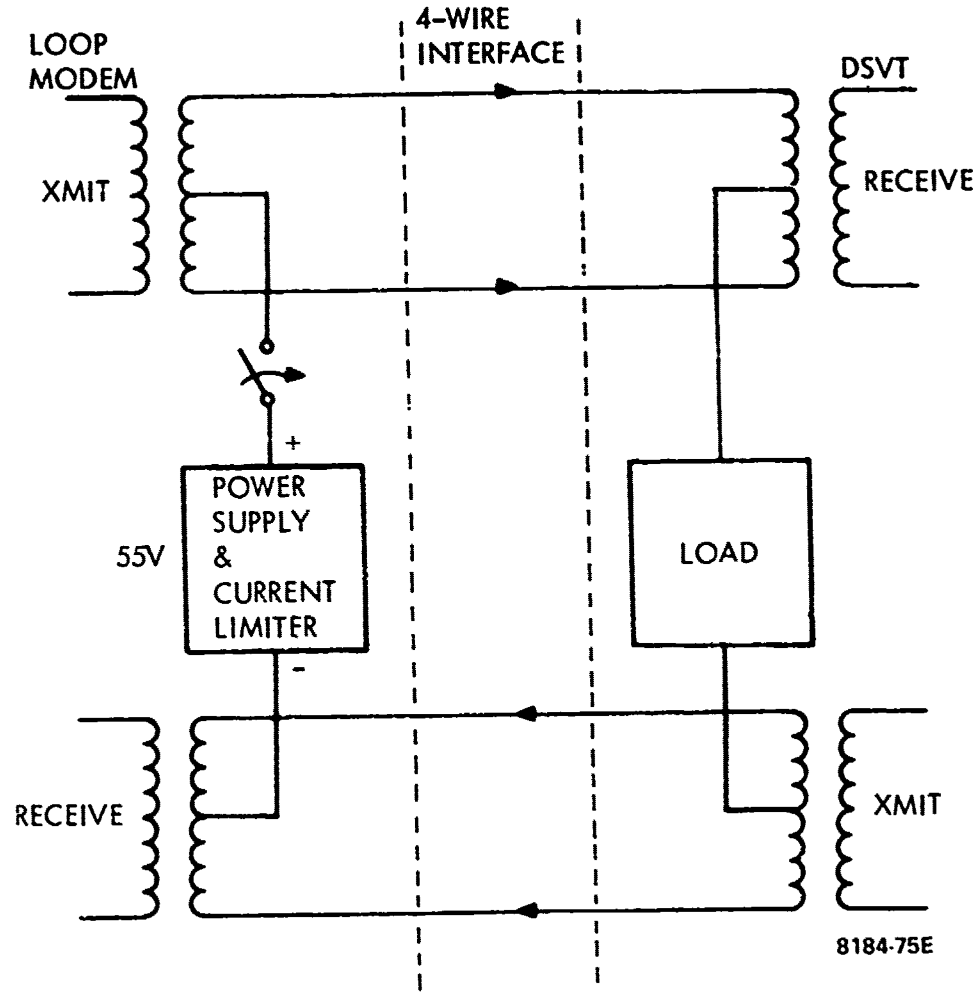


Figure 3-15. Phantom Loop Power Feed

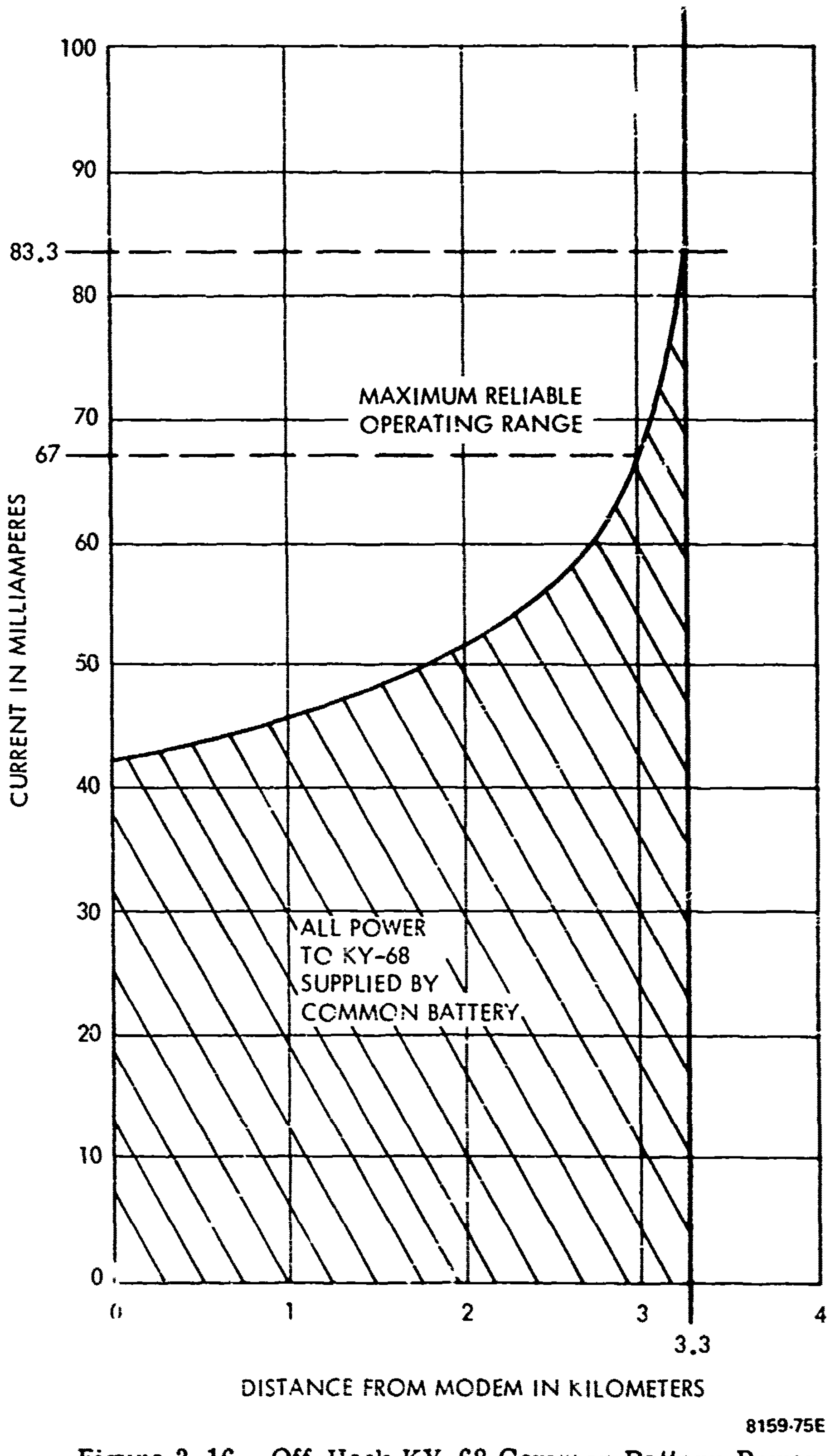


Figure 3-16. Off-Hook KY-68 Common Battery Power

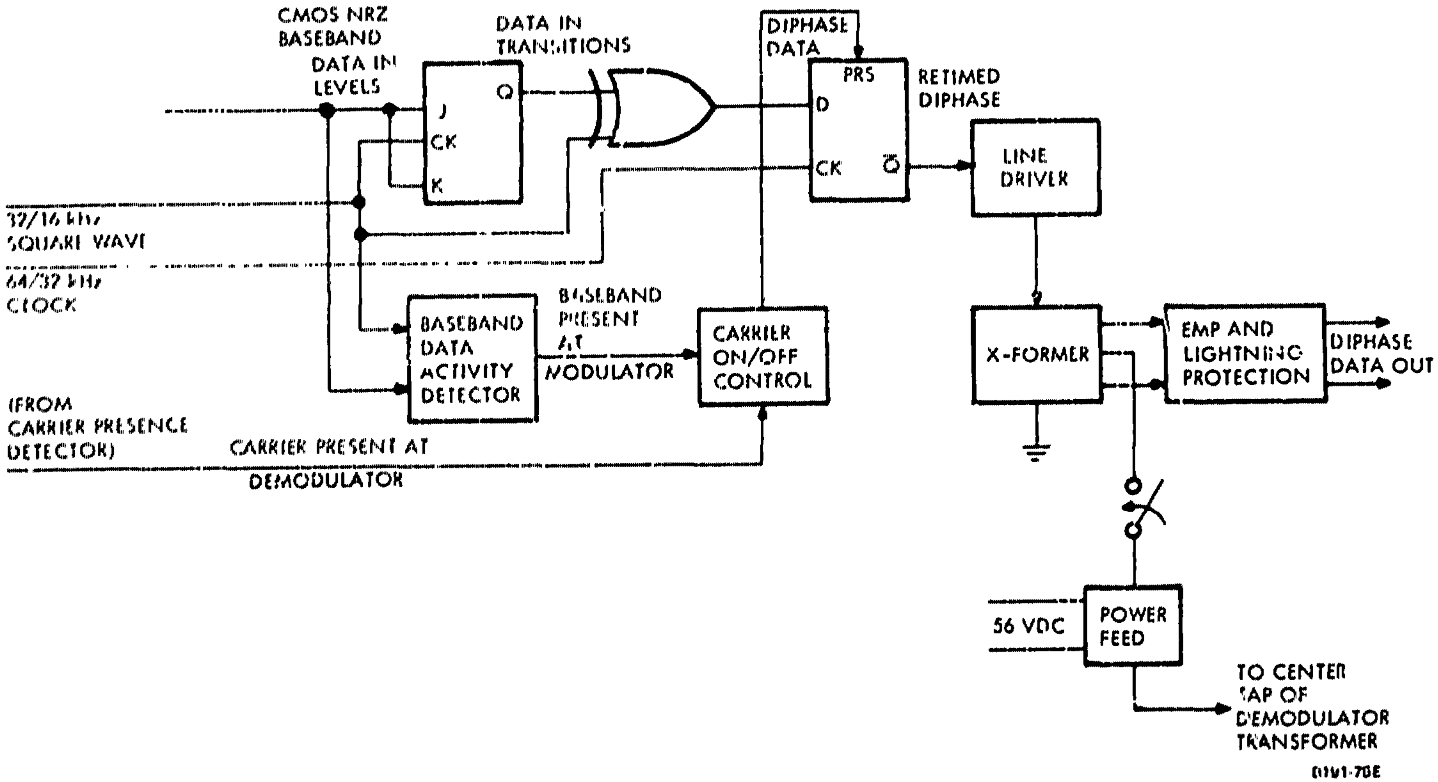


Figure 3-17. Loop Modem Modulator Section

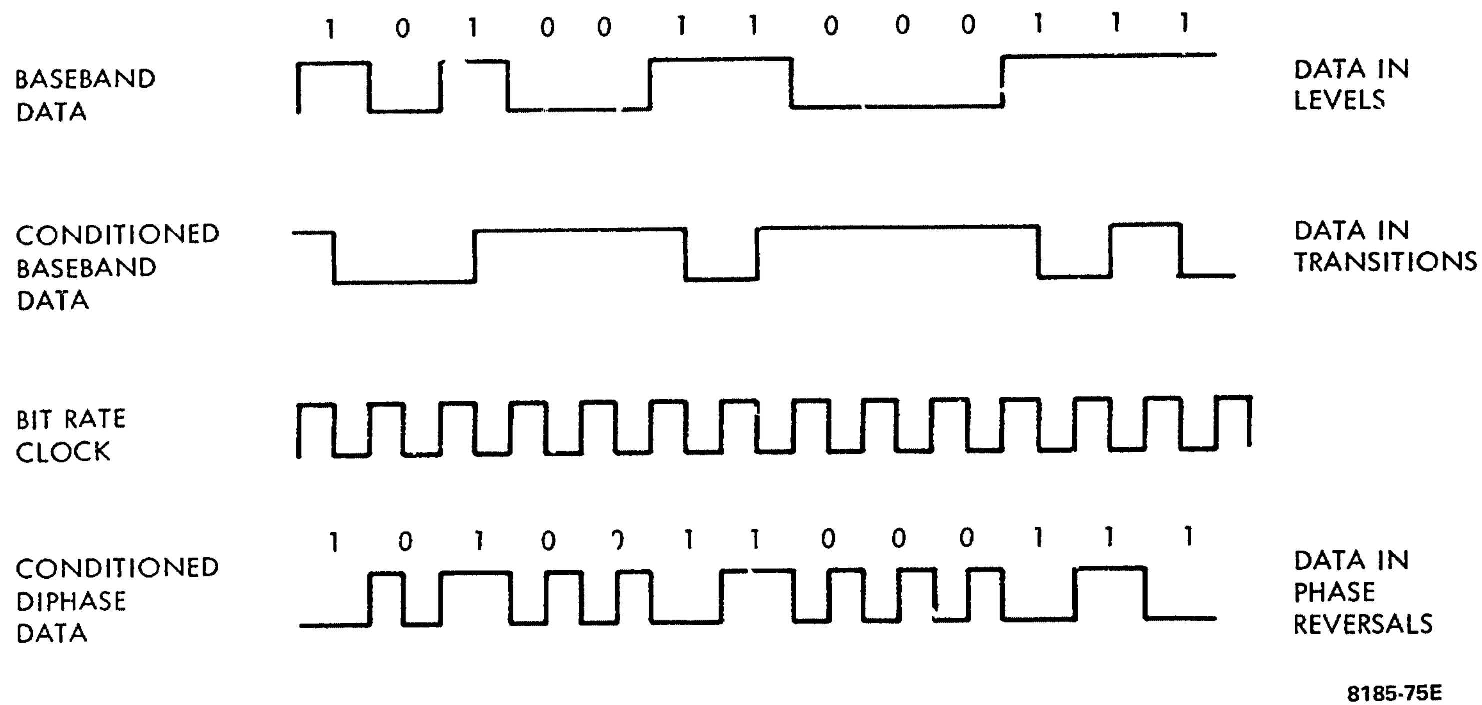


Figure 3-18. Generation of Conditioned Diphase Data

crosstalk and provide EMP protection to the line driver by filtering out hf, high level EMP transients. The transformer couples the line driver to the line. The signal level on the loop side of the transformer shall be 3.0 Vp-p ± 10%. The rise and fall times are nominally 5% of the bit period at 32 kb/s or 1.56 μsec. The rise and fall time remains 1.56 μs (10-90% nominal) when the bit rate is changed to 16 kb/s. The transformer provides 600V isolation between the line driver and line. The transmitted waveform is square with less than 5% droop.

3.3.5.2 Diphase Demodulator

Refer to Figure 3-19 for a block diagram of the diphase demodulator. The input transformer AC-couples the input diphase signal to the band limited amplifier. The minimum detectable signal level is 150 mV to prevent near-end crosstalk from interfering with receive operation. The comparator and level converter transform the received diphase to CMOS logic levels. The diphase is delayed by one half bit, by shifting it through an eight bit shift register. The delayed diphase is compared with the undelayed diphase, the resulting output is baseband return to zero data. The mark detector generates a pulse for each mark (one) in the baseband return to zero. When in sync the data sampling pulse from the 4-bit counter occurs at the same time as the pulses from the mark detector. If the pulses from the mark detector consistently occur at the wrong time, the starting count of the 4-bit counter is altered by one in the appropriate direction. This action will synchronize the data sampling pulse to the pulses from the mark detector. The data sampling pulses sample the baseband return to zero data. The data is converted to baseband NRZ and synchronized to the bit rate clock in the DATA retiming and synchronizer block.

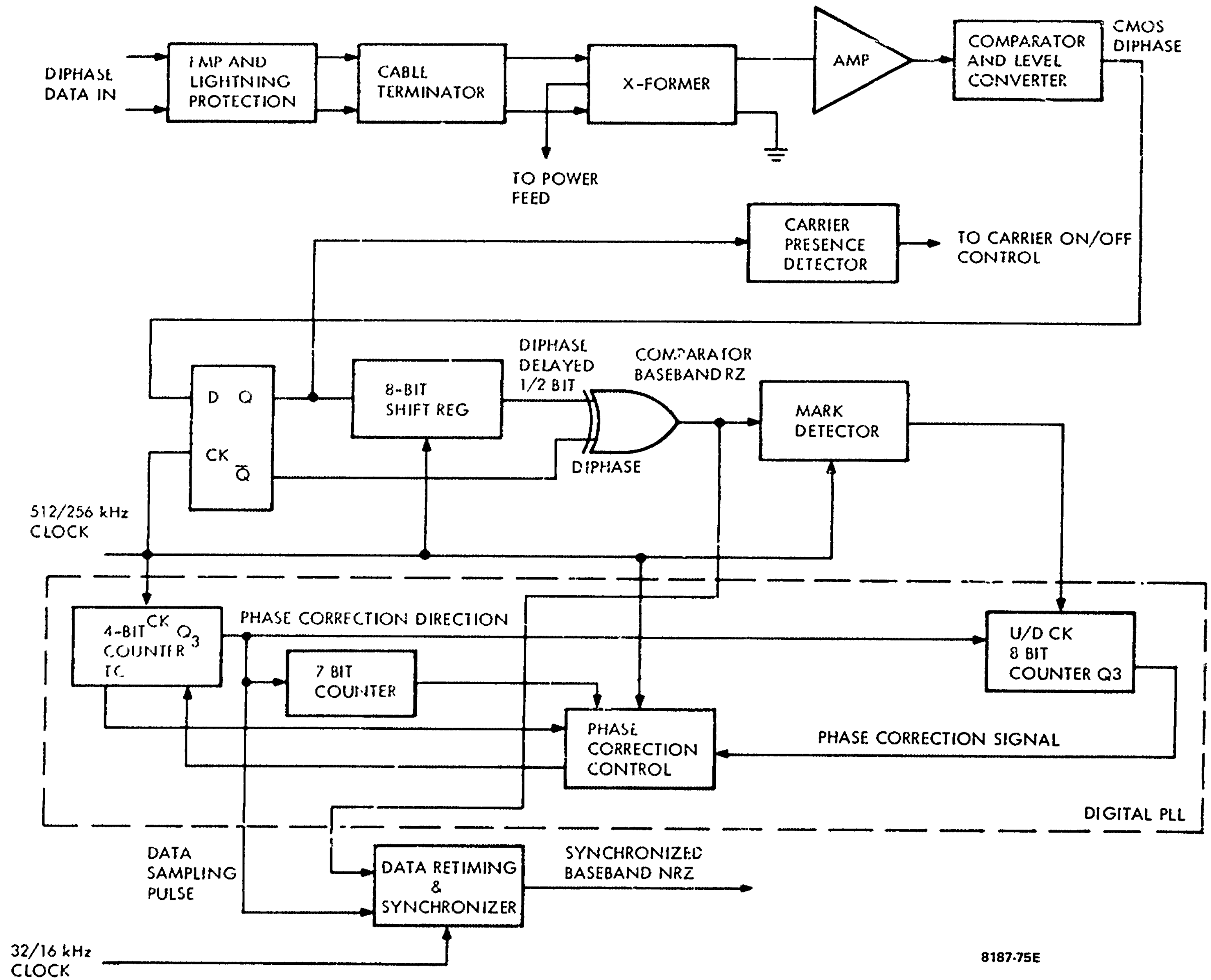


Figure 3-19. Loop Modem Demodulator Section

3.3.5.3 Phone Wake-up and Shutdown

Local Phone Initiating Call

DSVT	Loop Modem	Circuit Switch
1. Goes off hook; sends carrier and seize code	2. Sense carrier; Turn on Xmit carrier; send data to switch	3. Receive data send Seize acknowledge "dial tone"
4. Sends digits, etc. conversation		
5. Goes on hook; sends release code		6. Received release; sends all ones
7. Phone receives all ones; shuts off carrier	8. Loop modem sees all ones from switch and no carrier from phone; shuts off xmit carrier; sends all ones to switch	

Local Phone Receiving Call

DSVT	Loop Modem	Circuit Switch
3. Phone sees carrier activity sends ring acknowledge; conversation	2. Detects baseband activity; turns on Xmit carrier	1. Sends ring code
4. Goes on hook; sends release code		5. Receives release; sends all ones
6. Phone receives all ones; shuts off carrier	7. Loop modem sees all ones from switch and no carrier from phone shuts off Xmit carrier: sends all ones to switch	

3.3.6 Interface P.C.B./Interface Drivers and Receivers

3.3.6.1 Interface Card

The Interface card is used only in the LGM for the group interface of data and timing signals. The functional elements of the interface card are as follows:

1. Line Receiver for Group Data
2. Line Receiver for Group Clock
3. Line Driver for Group Data
4. Line Driver for Group Clock
5. FIFO Buffer

The Line Receiver consists of a AM1500 dual comparator; the Line Driver consists of a AM2616 quad driver; both are discussed in Section 3.3.6.2 below.

The Fifo Buffer is a 16 bit buffer (±8 bits) between the incoming group data and the group demultiplexer. The data is clocked into the buffer by the received clock and read out of the buffer by the Group clock internal to the unit. The buffer is centered by the "go to frame" pulse from the synchronizer.

A block diagram of the interface card is shown in Figure 3-20.

3.3.6.2 Interface Drivers and Receivers

A common balanced interface circuit will be used throughout the RMC, RLGM and LGM units. This circuit is shown in Figure 3-21 and consists of the following circuits.

- AM2616DM line driver
- LM2111D or AM1500 dual comparator
- 54LS04J HEX inverter
- CD4050A Level converter

These devices will be used to convert the C-MOS signals to compatible balanced interfaces and vice versa.

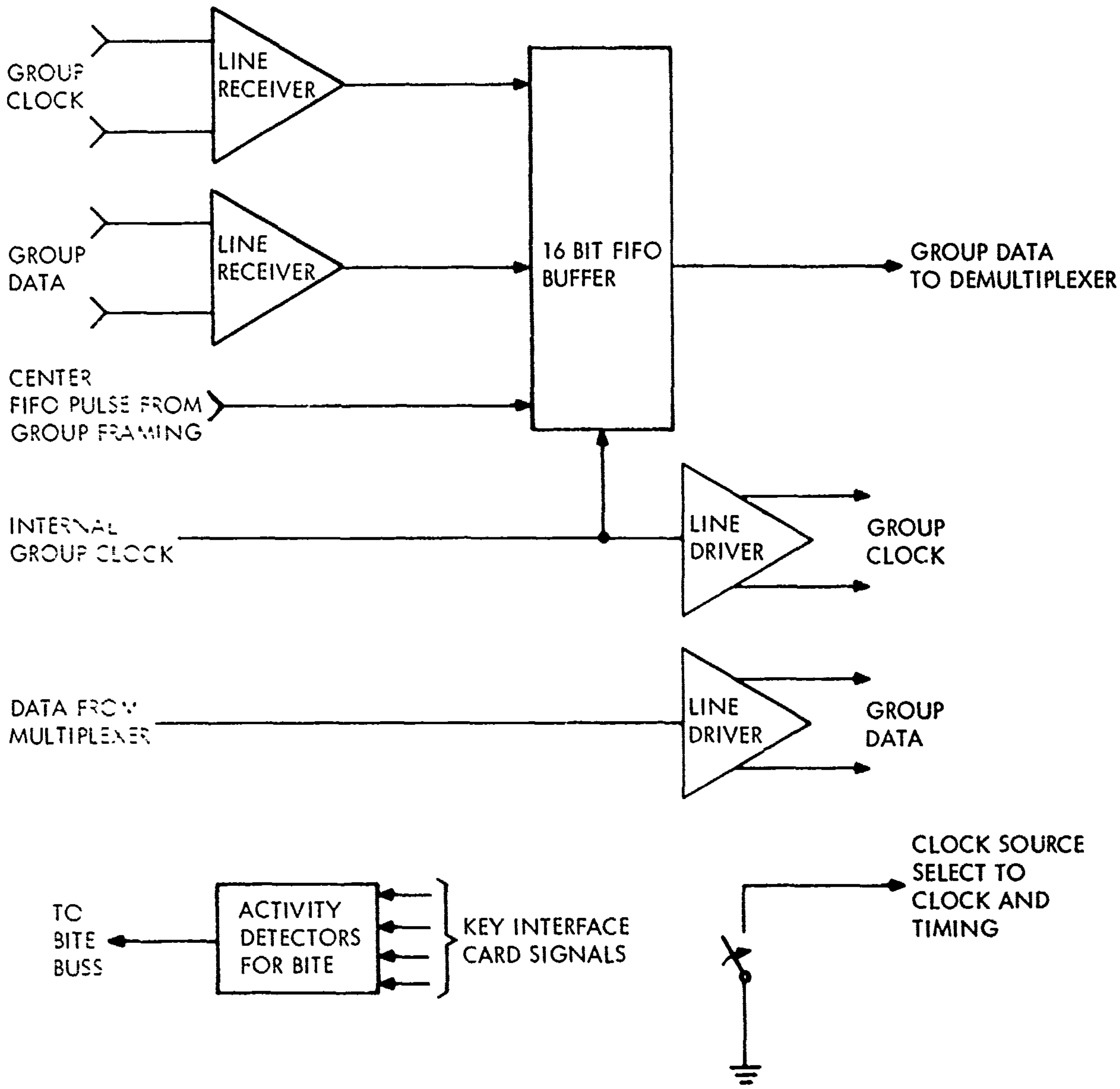


Figure 3-20. Interface Card Block Diagram

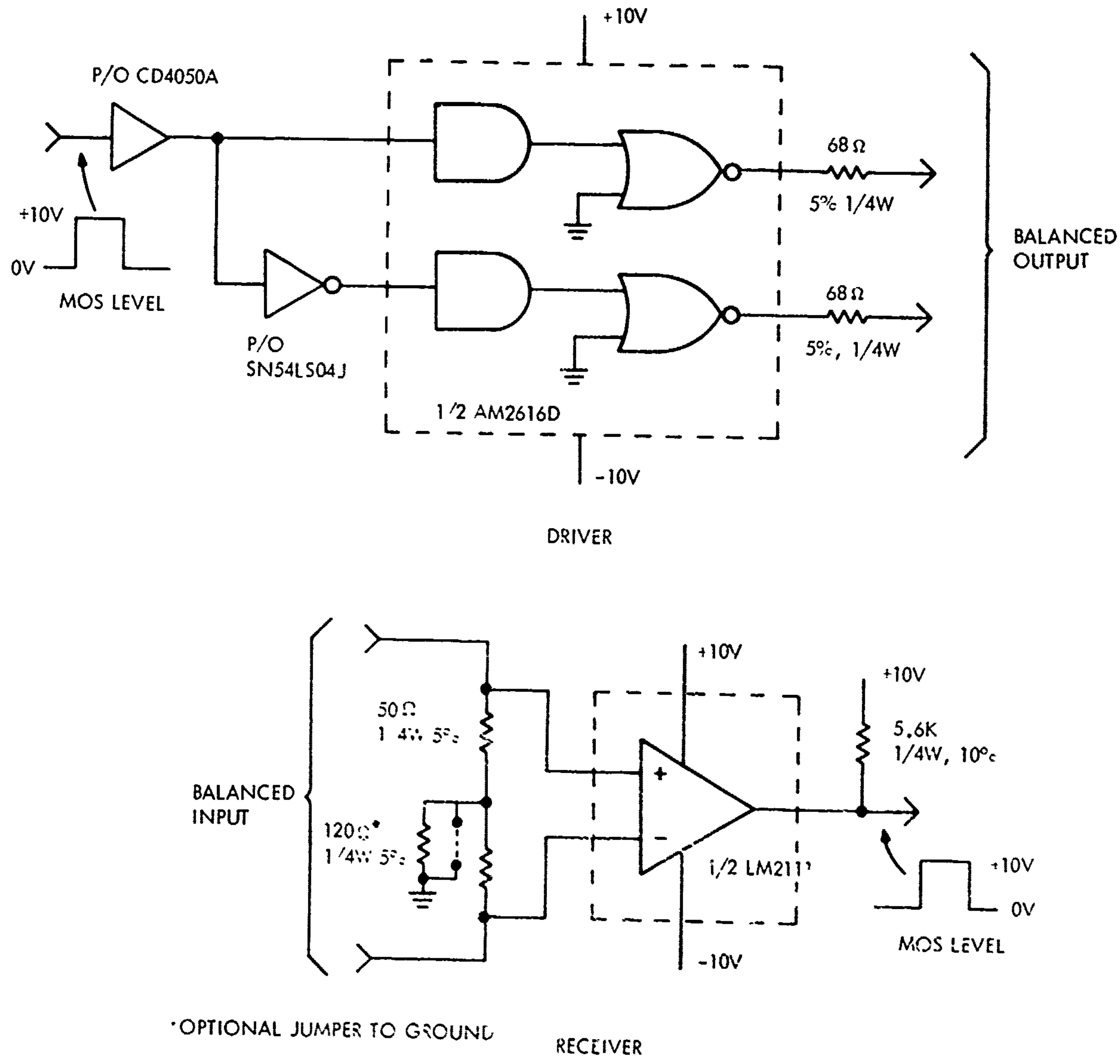


Figure 3-21. Balanced Interface Circuit

Converters are packaged on the P. C. B.'s generating specific functions (e.g., LGM group data on the Interface card).

Table 3-7 shows the P. C. B.'s which contain the balanced drivers and receivers. Table 3-8 shows the interface lines within each unit which contain the balanced drivers and receivers.

Several lab tests were run on the Advanced Micro Devices type AM2616 line driver to determine its characteristics.

TABLE 3-7. NRZ BALANCED INTERFACES BY CIRCUIT CARD

- Interface

  2 Drivers (Transmit Group Data; Transmit Group Clock)

  2 Receivers (Receive Group Data; Receive Group Clock)

- Timing Generator

  3 Drivers (Telemetry Data Out; Telemetry Clock Out; Sync Command)

  3 Receivers (Frame Squelsh; Telemetry Data In; Sync Achieve)

- Loop Modem

  None

- Group Modem

  None

- Group Framing

  None

- MUX/DEMUX

  None

- BITE

  None

TABLE 3-8. NRZ BALANCED INTERFACES BY EQUIPMENT

RLGM

- Station Clock (Input)

RMC

- Station Clock Input

LGM

- TED Control (Out)
- Group Data (In/Out)
- Group Transmit Clock
- Group Receive Clock
- Telemetry Data (In/Out) (2 kb/s)
- Telemetry Clock (Out) (2 kb/s)
- Station Clock (In)

TEST 1.

In the first test, the circuit in Figure 3-22 was constructed, and various values of R_L were placed in the circuit. The positive and negative peak values of volts out (VO) were recorded for each value of R_L (Table 3-9). The peak load current (I_L) was then calculated for each value of R_L. The results of these measurements were plotted in Figure 3-23, the AM2616 output characteristics. Several representative load lines were then drawn and as shown in Figure 3-23 this characteristic can be used to choose an operating point for the device.

TEST 2.

Figure 3-24 illustrates the actual balanced driver-receiver circuit employing the AM2616. The load consisted of 50 ft. of number 24 shielded twisted pair line terminated in 100Ω. The value of R_S was selected to fall within the output characteristics in Figure 3-23, and to meet the driver output resistance and balance specifications.

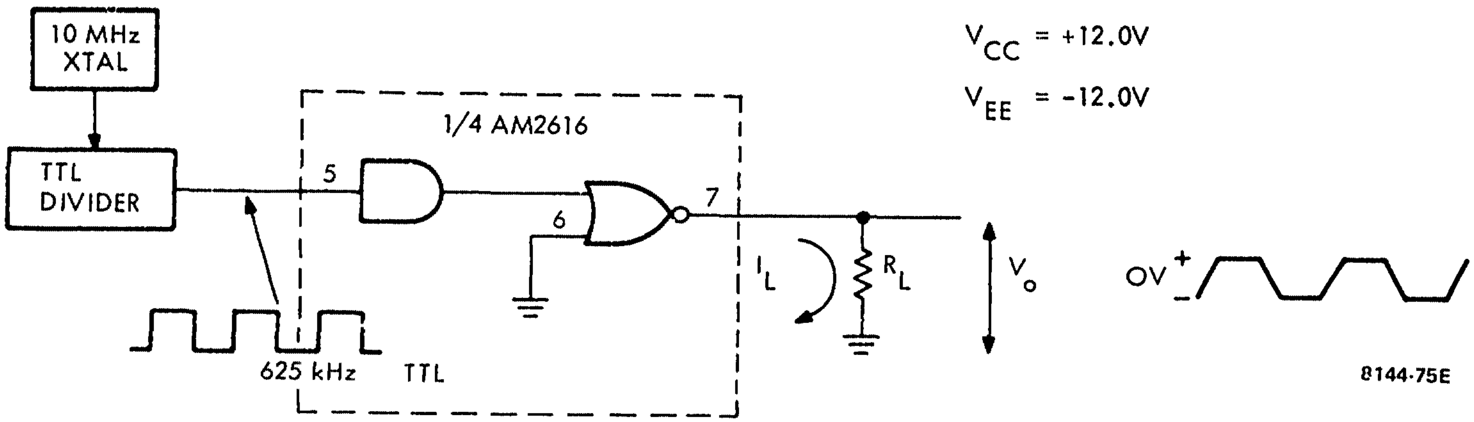


Figure 3-22. Interface Circuit

TABLE 3-9. R_L POSITIVE AND NEGATIVE PEAK VALUES

R_L	V_O	I_L
(Ω)	(Volts)	(mA)
22.8	+0.40 -0.40	+17.5 -17.5
49.0	+0.8 -0.9	+16.2 -18.3
94.0	+1.6 -1.7	+17.0 -18.1
148.0	+2.5 -2.7	+16.9 -18.2
183.7	+3.2 -3.3	+17.4 -18.0
270.0	+4.6 -4.7	+17.0 -17.4
307.0	+5.2 -5.4	+17.0 -17.6
327.0	+5.5 -5.7	+16.7 -17.5
353.0	-5.5 -5.6	+15.6 -16.1
464.0	+5.9 -6.1	+12.7 -13.1
859.0	+6.0 -6.1	+ 7.0 - 7.1
1.45k	-6.1 -6.2	+ 4.2 - 4.3
2.70k	-6.2 -6.2	+ 2.3 - 2.3
3.34k	+6.3 -6.3	+ 1.9 - 1.9

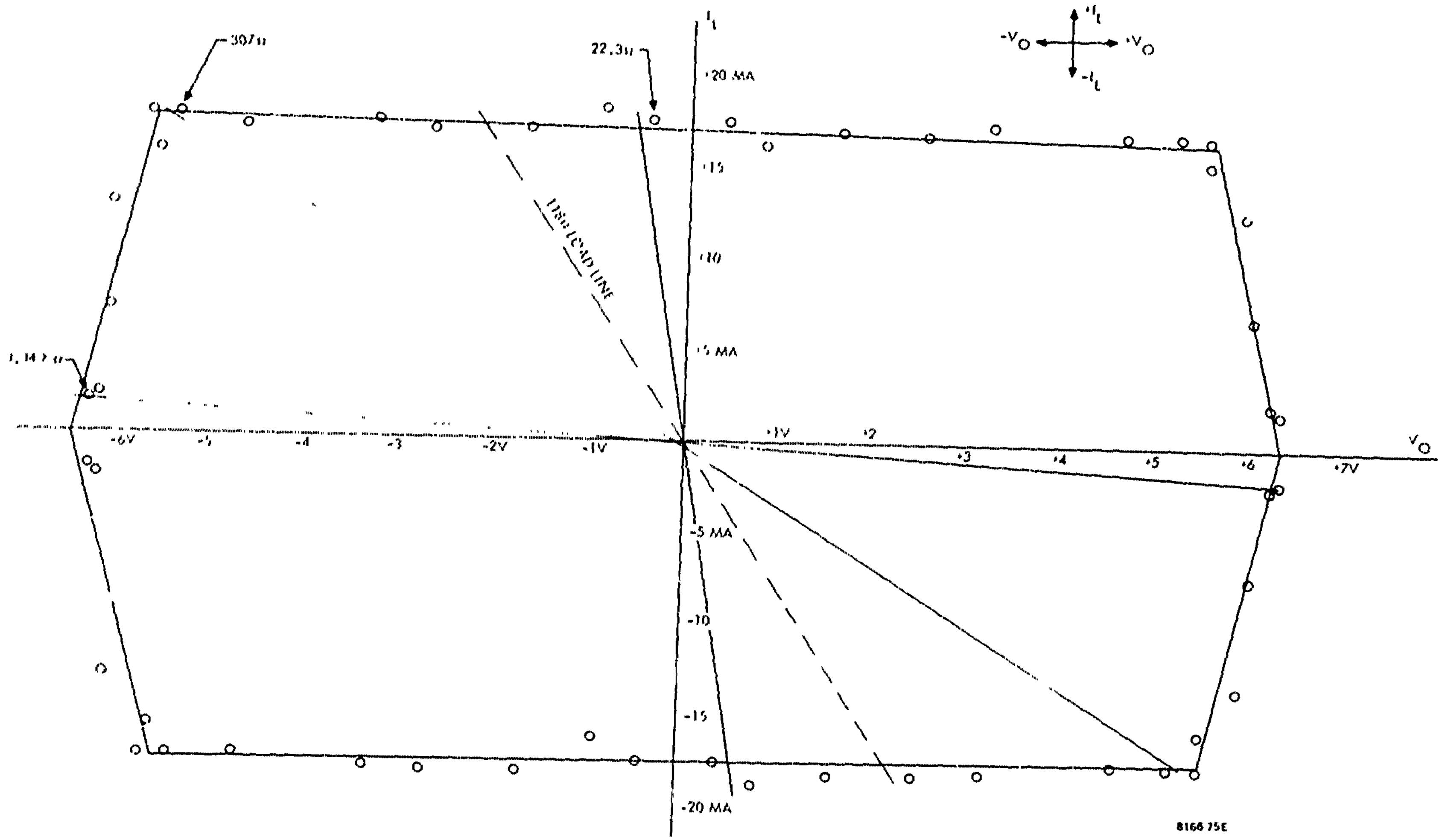


Figure 3-23. AM2616 Output Characteristics

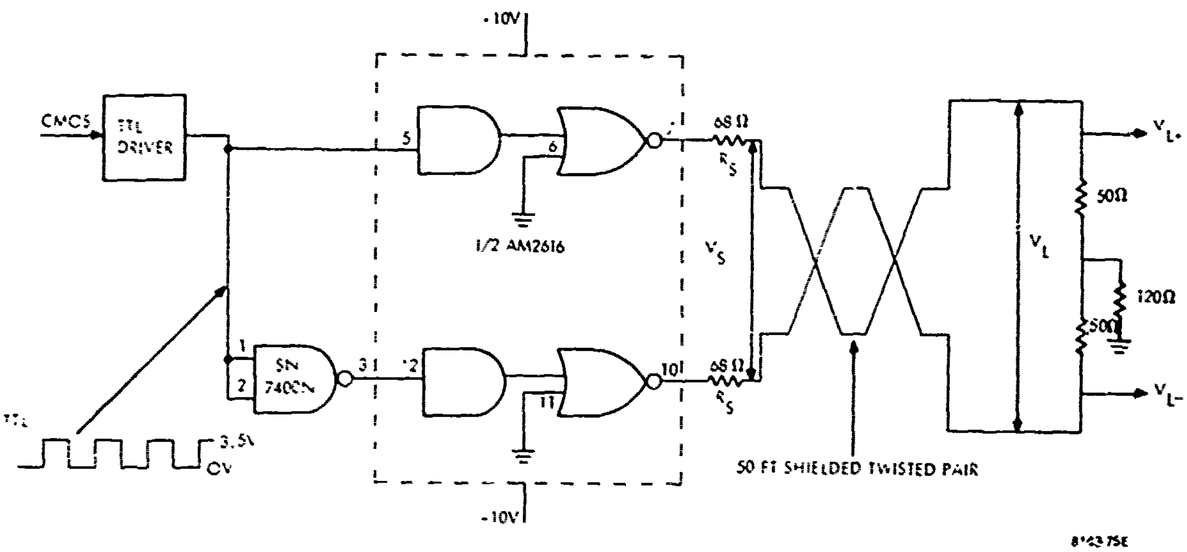


Figure 3-24. Driver Circuit Employing AM2616

TEST 3.

The AM1500 voltage comparator was employed as the receiver. The output of this device will drive CMOS.

The circuit in Figure 3-25 was tested for the following requirements:

- Driver output voltage
- Receiver input sensitivity
- Performance in the presence of noise
- Protection - (this included connecting both lines of the twisted pair to +10V or -10V for 1 second; no damage resulted).

The test conducted on these circuits suggested that they could be used for the interface as specified in Paragraph 4.3.1.3.3.9 of MIL-STD-188-100 with the exception of the 25 volt protection requirement. The AM2616 device was tested to a constant voltage of 10 volts across its output terminals without damage. To protect this circuit for 25 volts would require eight (8) additional components consisting of diodes and resistors and would dissipate

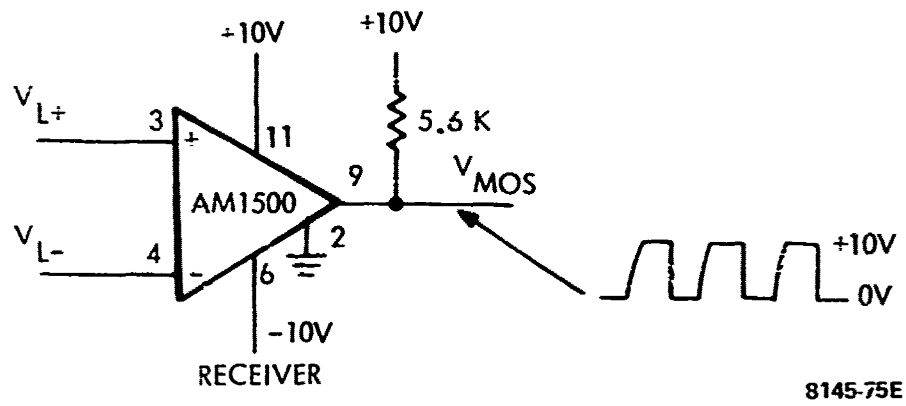


Figure 3-25. AM1500 Receiver Circuit

about 12.5 watts under a fault condition. Based on the weight and power constraints of each unit, it was concluded that the 10 volt limit is consistent with good design practices and that the additional hardware required to protect the circuits for 25 volts was not warranted.

Features of the AM2616 and AM1500 are listed in Table 3-10.

3.3.7 BITE LGM

Refer to Paragraph 5.3.7 of this volume for the detail description of the BITE P.C.B.

TABLE 3-10. AM2616 AND LM2111D FEATURES

AM2616 Line Driver (SM-A-838096)

- Dual - In - Line Package
- Short Circuit Protected Output
- Internal Slew Rate Limiting
- Supply Independent Output Swing
- Output Impedance Guaranteed Less than 100Ω
- Used in TTC-39 Equipments
- Guaranteed to Survive ±15V Applied to Outputs

LM2111D/AM150031E Voltage Comparator (Line Receiver)

- Dual - In - Line Package or Metal Can, Full Temperature Range
- Single or Dual Units
- M.O.S. Compatible Output
- Maximum Differential Input ±30V
- 10 μv Sensitivity
- Guaranteed to Survive Input Voltages Up to the Supply Voltage
- Available From Advanced Micro Devices, National and Signetics

3.3.8 Power Supply

3.3.8.1 Introduction

The Power Supply design represented a most significant technical challenge. The power supplies must have efficiencies of as high as 65% while at the same time be constrained within tightly controlled space and weight restrictions. For this reason, an extensive make/buy evaluation was undertaken. In this regard, there was generated a detailed power supply specification SM-A-876875 and Statement of Work. This power supply specification was submitted to ECOM.

3.3.8.2 LGM Power Supply Design

3.3.8.3.1 Major Perforr ice Requirements

The voltage and current requirements between the RLGM, RMC and LGM are very closely related. There is, therefore, a common specification requirement for both the shelter and field units. This similarity has resulted in a high degree of Power Supply commonality which has resulted in the utilization of common P.C.B.'s in each of the three units. A total of six P.C.B.'s are required for these units. Table 3-11 shows the utilization, type, and electrical requirements of these modules.

Other performance requirements of the Power Supply are summarized in Table 3-12. These requirements are described in the Power Supply specification SM-A-876875.

TABLE 3-11. GTE SYLVANIA POWER SUPPLY P.C.B. COMPLEMENT

Module Type	Used In	Output Voltages	Current (Amps)	Overvoltage	Overcurrent (Amps)
A	LGM	+5 -5 +10 -10	2.0 to 3.0 1.5 to 2.0 0.8 to 1.0 0.8 to 1.0	5.9 to 6.5 -5.9 to -6.5 11.4 to 12.6 -11.4 to -12.6	3.25 2.25 1.2 1.2
D	RMC	+55 +180	0.75 0.3	58 200	1.65 0.35
H	LGM, RLGM	+55	0.085 to 1.5	58	1.65
J	RMC, RLGM	+5 -5 +10 -10	1.0 0.15 1.0 0.15	5.9 to 6.5 -5.9 to -6.5 11.4 to 12.6 -11.4 to -12.6	22.5 Watt Limit
B	LGM, RMC, RLGM	- Contains the internal supply and pre-regulators			
C	LGM, RMC, RLGM	- Contains the DC/DC converter, nuclear shutdown sensor, and fault logic			

TABLE 3-12. MAJOR PERFORMANCE REQUIREMENTS OF POWER SUPPLY

	LGM	RLGM	RMC
• Input Power Source			
1. 120 Volt, Single Phase, 47 to 420 Hz	X	X	X
2. +28 Volt DC	X	X	X
3. +180 Volt DC		X	
• EMP/Lightning Protection		X	X
• Automatic Input Power Detector (AC/DC)	X	X	X
• Reverse Polarity Protection	X	X	X
• Power Supply Efficiency			
1. AC Operation - 75%	X	X	X
2. DC Operation - 65%		X	X
• Overvoltage Protection for All DC Outputs	X	X	X
• Radiation Detector for Crowbarring all DC Outputs	X	X	X
• Overcurrent Protection for all DC Outputs	X	X	X
• Short Circuit Protection for all DC Outputs	X	X	X
• Multiple DC Outputs			
1. -5 Volts	X	X	X
2. -5 Volts	X	X	X
3. +10 Volts	X	X	X
4. -10 Volts	X	X	X
5. +55 Volts	X	X	X
6. +180 Volts			X
• Special (+180 Volt) Overcurrent Requirement			X
• Special (+180 Volt) Undercurrent Protection			X

TABLE 3-12. MAJOR PERFORMANCE REQUIREMENTS OF POWER SUPPLY (Cont.)

	LGM	RLGM	RMC
• Internal Power Monitor Circuits	X	X	X
• Power Coupling Circuits to CX-11230 Cable		X	X
• Natural Convection Cooling	X	X	X
• Reliability - Minimum 25,000 Hrs. MTBF	X	X	X
• Ambient Temperatures			
1. Operating -32°C to 63°C	X		
2. Non-Operating - 57°C to 71°C	X		
3. Operating -46°C to 71°C		X	X
4. Non-Operating -57°C to 71°C		X	X
• Environmental Requirements			
1. Humidity	X	X	X
2. Altitude (Operating 10,000 Feet)	X	X	X
3. Dust	X	X	X
4. Salt Fog	X	X	X
5. Fungus	X	X	X
6. Vibration	X	X	X
7. Shock	X	X	X
8. Acoustic Noise	X	X	X
9. Four Foot Drop Test		X	X
• Parts, Materials, and Processes per MIL-P-11268	X	X	X
• EMI Filter Internal to Supply		X	X
• S&V Design Guidelines	X	X	X

3.3.8.3.2 Functional Description

A flyback type of converter is used for the DGM power supplies. This type of converter has been used quite extensively in space applications where high reliability and efficiency is a must. Before details of the DGM power supplies can be discussed, a brief description of the basic flyback operation would be beneficial.

A schematic depicting a flyback converter is shown in Figure 3-27, and a brief discussion of this type of converter follows.

Transistor Q1 is turned on by the driver circuitry which causes current to flow through T1. However, diode CR2 is reverse-biased during this period allowing flux to build up in T1. When the collector current reaches a predetermined point, transistor Q1 turns off allowing the flux built up in the core to collapse, which in turn forward-biases CR2 allowing current to flow to C1. The energy stored in the core is given by the equation:

$$E = 1/2 \, Li^2$$

Therefore, the amount of energy stored is proportional to the square of the collector current. Likewise, the voltage output is given by the equation:

$$Eo = E_{IN} \frac{(N2)}{(N1)} \frac{(\Delta t \text{ on})}{(\Delta t \text{ off})}$$

Output voltage regulation is achieved by monitoring the voltage by an error amplifier and using this output to set the amount of current to turn Q1 off. Therefore, the output voltage is regulated by adjusting the amount of power transferred by T1.

Output filtering is achieved by T1 secondary and C1. The rate of flux collapse is controlled by output voltage, L formed by the secondary winding, and C1. Additional filtering can be achieved by adding additional L and C networks.

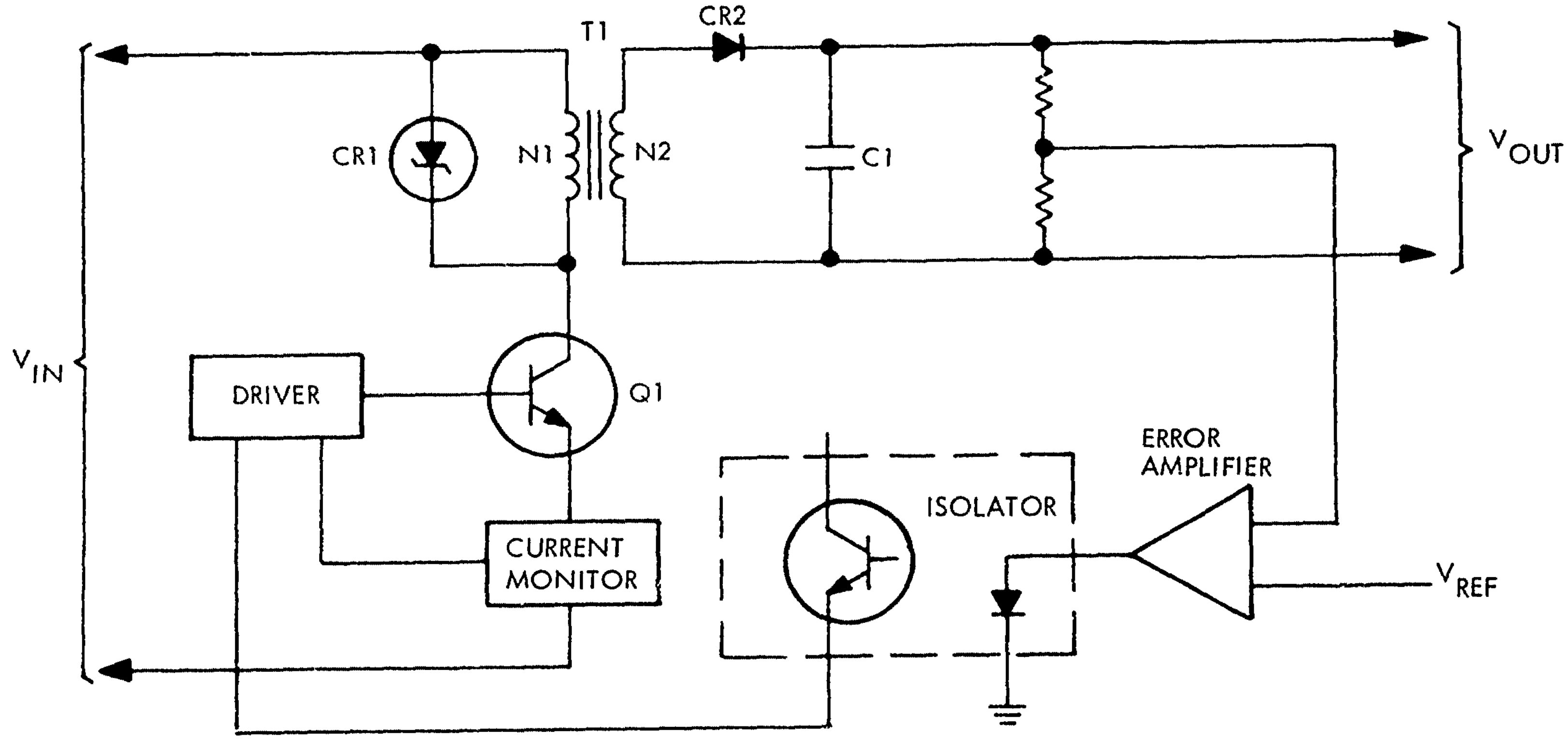


Figure 3-26. Flyback Converter

This type of converter exhibits some interesting protection characteristics.

By storing energy introduced on one-half cycle through winding N1 and then delivering this energy to the load through winding N2 on the next half cycle, the circuit of Figure 3-26 functions as a DC to DC voltage converter. A major difference between this method of voltage conversion and more conventional methods is that the extraction of energy from the source and the delivery of energy to the filter capacitor and load occur on opposite half cycles. This fact has considerable significance insofar as protecting transistor Q1 and diode CR2 from current transients caused by load short circuits is concerned.

Current limiting can be done by simply limiting the maximum collector current allowed to pass through Q1.

The LGM power supply is comprised of modular blocks utilized extensively in the DGM family. A block diagram of the LGM power is shown in Figure 3-28.

Prime power having been pre-conditioned by EMI filters and EMP arrestors external to the unit is routed to the AC input network. Figure 3-28 is a schematic of this circuit. A two pole circuit breaker is used on the input. The circuit breaker will break both sides of the line, but senses only the hot side of the line. Trip points are set at 3 amps RMS for the 115V AC operation. Figure 3-28 shows the circuit breaker configuration.

AC is rectified into a nominal 160 VDC. This high voltage is applied as source power to the flyback converters of the "B" and "H" modules which provide regulation and input/output isolation.

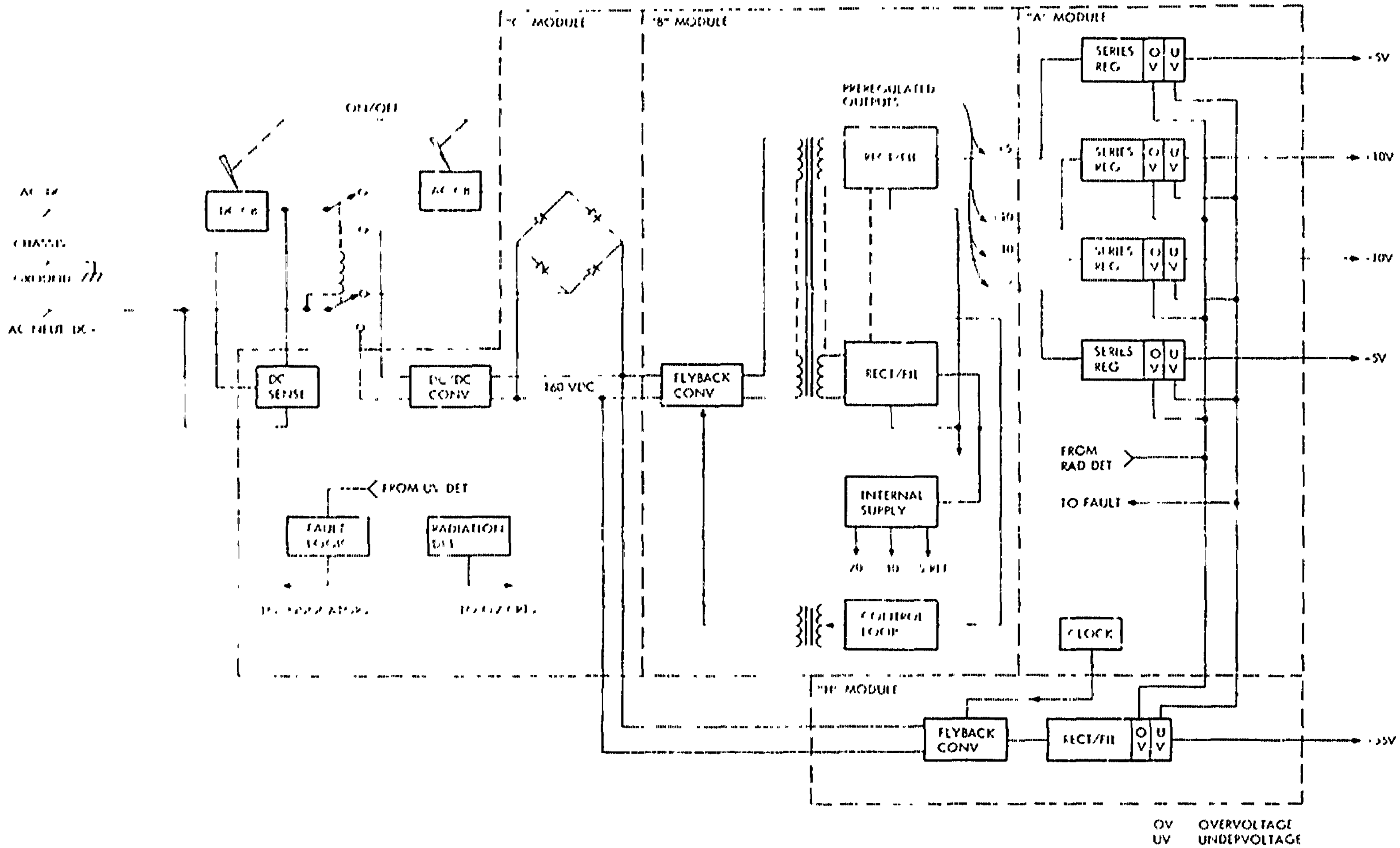


Figure 3-27. LGM Power Supply Block Diagram

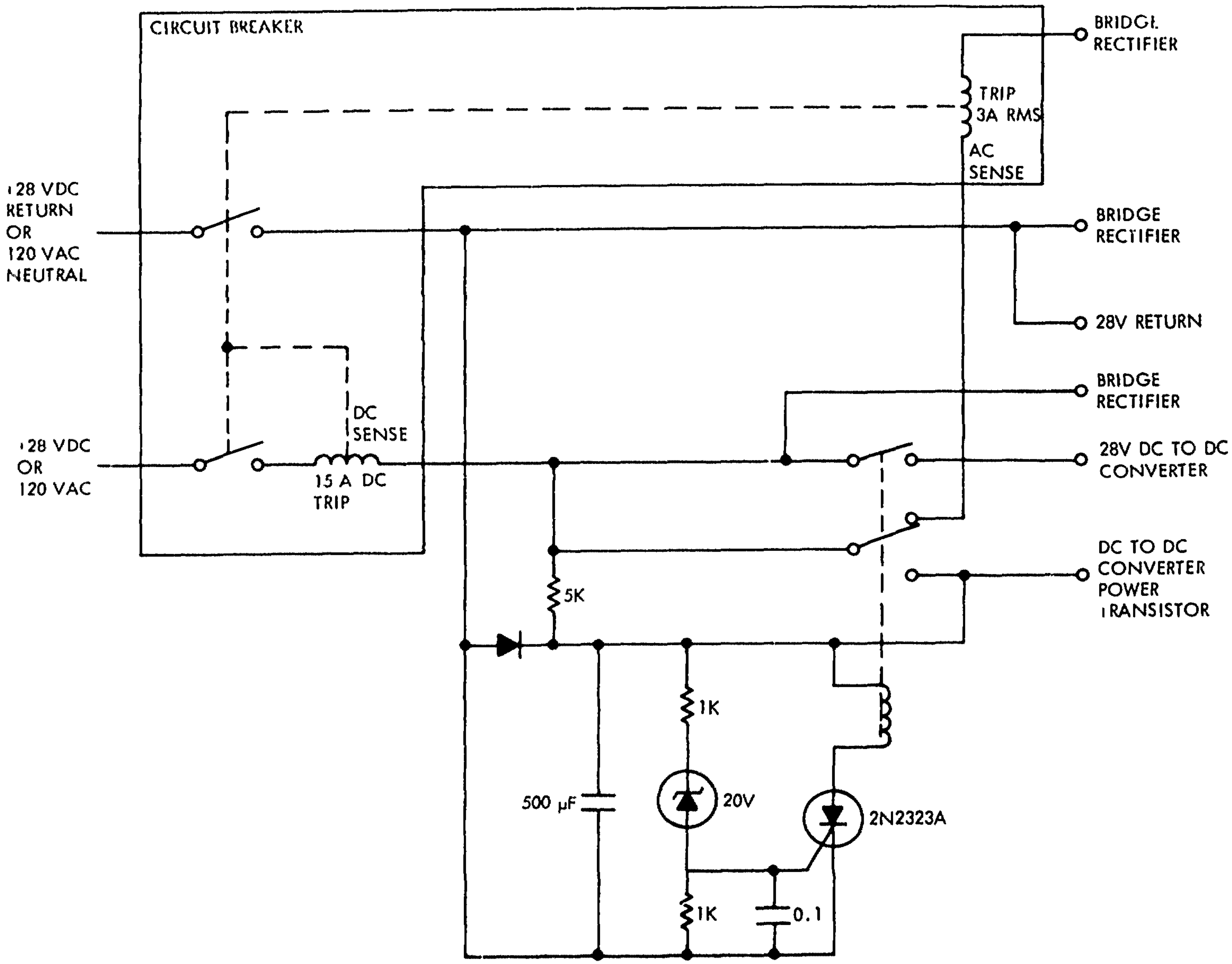


Figure 3-28. Prime Power Detector and Circuit Breaker Diagram

The "B" module converter transforms the high voltage (160V) DC into pre-regulated DC outputs for subsequent utilization as load supplies, internal bias supplies, or regulation loop control. The "H" converter, converts the 160V input to a regulated +55 VDC for transmission as source power to the DSVT's. Various operating conditions such as over and under voltage are monitored.

The local utilizing load supplies are further conditioned by series regulators and monitored for out-of-tolerance performance and subsequent indication.

Each output status is reported via the undervoltage (UV) summary combiner of the fault logic circuit. An overvoltage (OV) condition is crowbarred to protect the utilizing load and consequently appears as a UV anomaly following cessation of the OV indicated output. Impinging radiation is detected by a radiation circuit which initiates all crowbars, internal and external, to safeguard the load and the power supply.

3.3.8.3.3 PC Card Complement

The power supply modules which are used in the LGM are as follows:

Module Type	Function
A	Consists of four (4) series pass regulators for the +5 VDC and the +10 VDC, overvoltage circuits, undervoltage circuits, a clock and a power down circuit.
B	Consists of the internal supply and pre-regulators for the series pass supplies.
C	Consists of the radiation detector, and fault logic components.
H	Consists of the 55V DC at 1.5 amp circuitry

.3.8.3.4 Technical PC Board Description

.3.8.3.4.1 Module "C"

The card, shown schematically in Figure 3-29, contains the AC bridge recfier, the DC/DC converter, the fault logic, and the radiation detector. This card as originally designed to handle DC as well as AC prime power. The DC input equirement has been dropped for the LGM but still applies for the RMC and RLGM

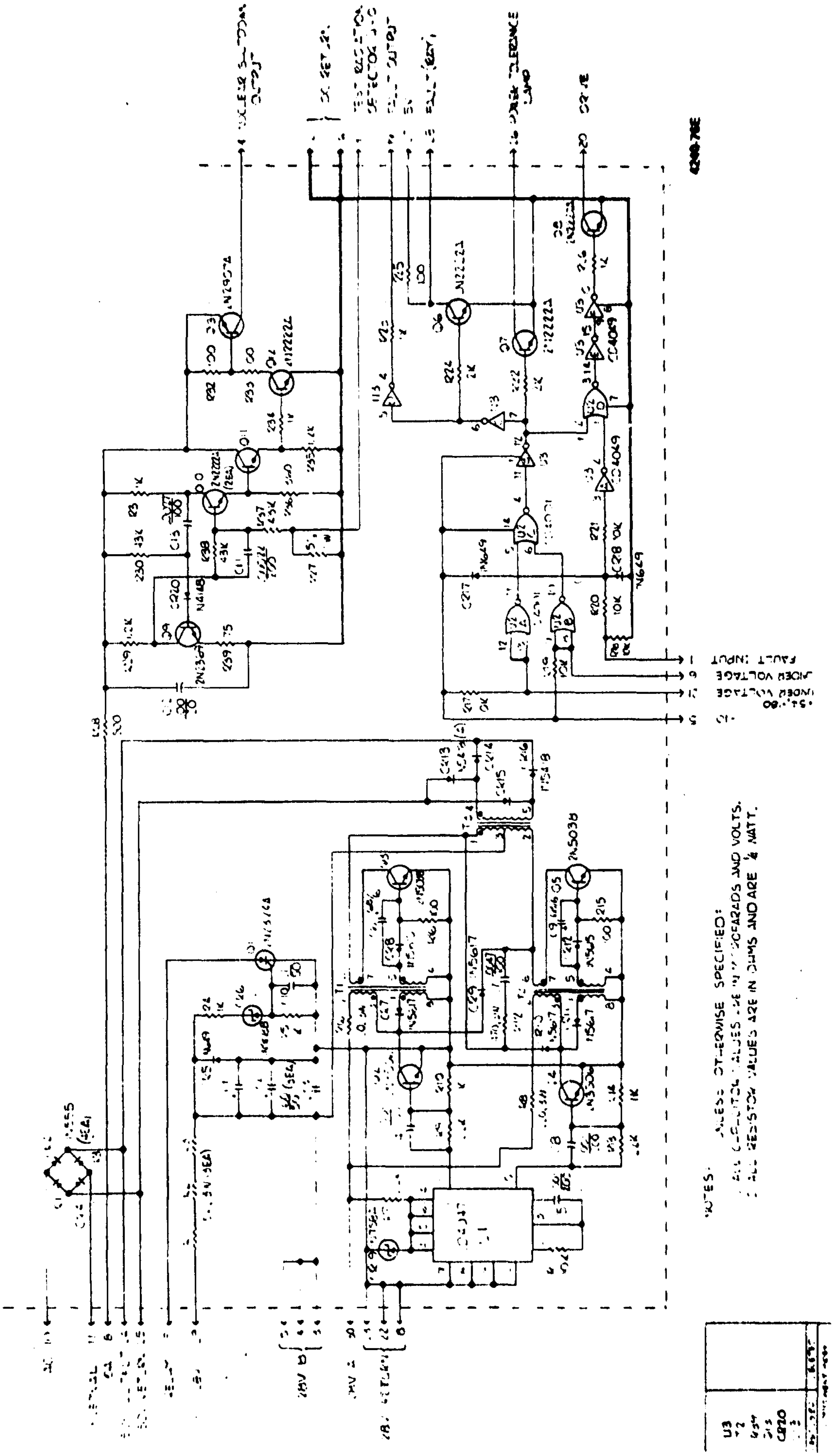


Figure 3-29. Power Supply, Module C

Best Available Copy

units. The C module is common to all three units and the circuit description which follows discusses DC as well as AC operation. The DC/DC converter is relatively straightforward, although it incorporates a feedback drive with clocked turn-off to facilitate efficiency in drive power and to minimize filter size by guaranteeing a fixed chopping frequency. An interlock assures simultaneous conduction does not occur.

The radiation detector is enabled when the 2N2222 conducts under nuclear bombardment, triggering and monostable. The fault logic combines the UV and test inputs to control the fault relay, fault lamp and power tolerance lamp.

3.3.8.3.4.2 Module "B"

The schematic in Figure 3-30 depicts the flyback converter with its associated control loop and the resultant regulated outputs. This converter employs proportional base drive for efficiency and clocked cycle drive for frequency stability. Source overvoltage protection inhibits operation under input voltage duress and a startup circuit provides reliable initiation. The basic tenet is that energy stored in the primary inductance of the transformer during conduction of the power transistor is transferred to the secondaries when conduction ceases in response to either the regulation loop on a high current sensor. Thus, the circuit is energy limited and behaves, in principle, like the "electric ram".

The secondary outputs are rectified and filtered: some supply the loads, one is used for control feedback, and one generates the +20V, +10V, and +5V reference utilized for internal bias and control.

3.3.8.3.4.3 Module "A"

Figure 3-31 illustrates the current limited series regulators with over-voltage (OV) crowbars and UV comparators. A clock generator for driving the "H" module and a power down circuit are located on this board. Adverse bias conditions in a radiation environment cause the supply to shut down. Note all crowbars are alternatively controlled by a signal from the radiation detector.

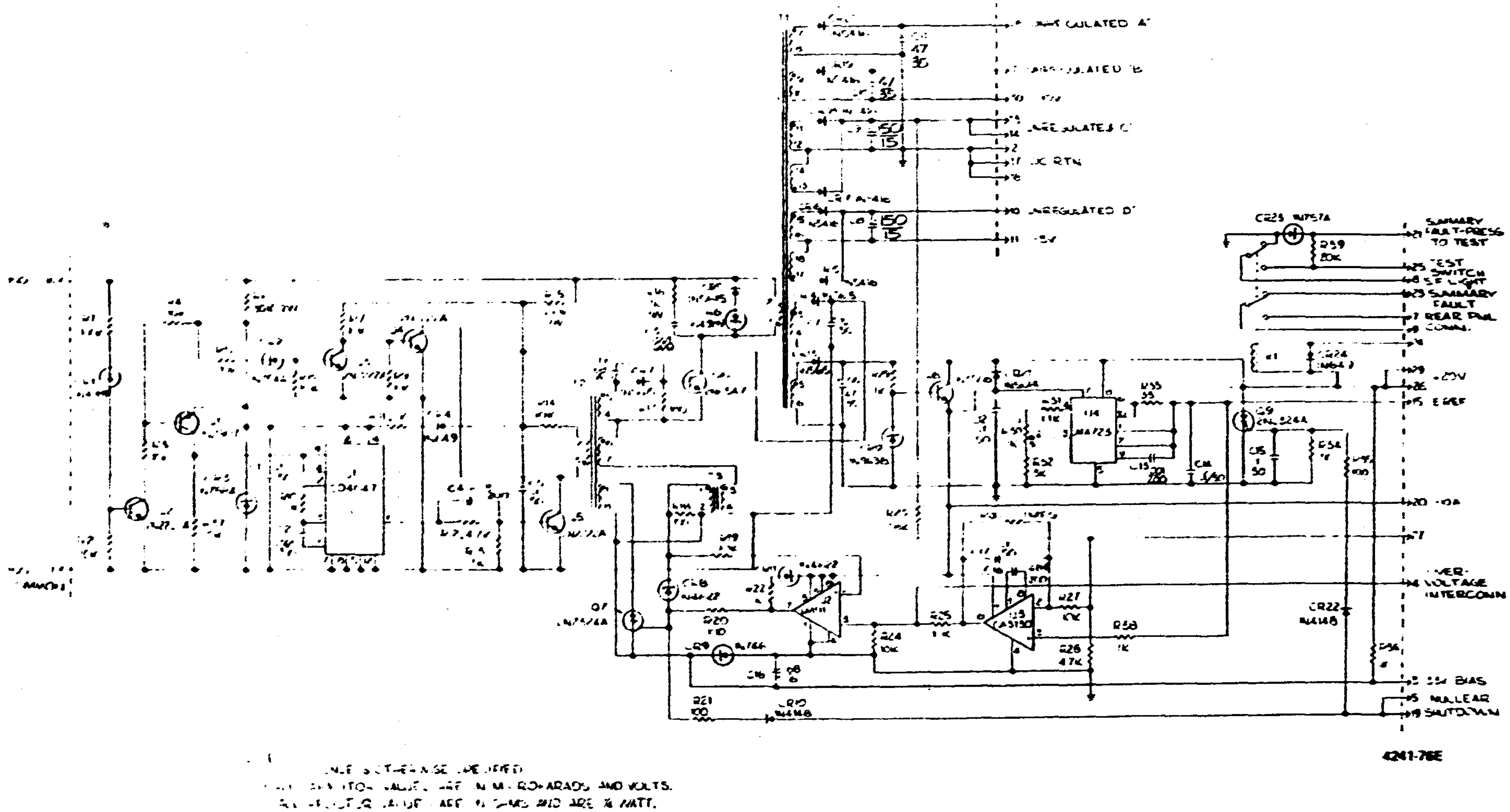


Figure 3-30. Power Supply, Module "B"

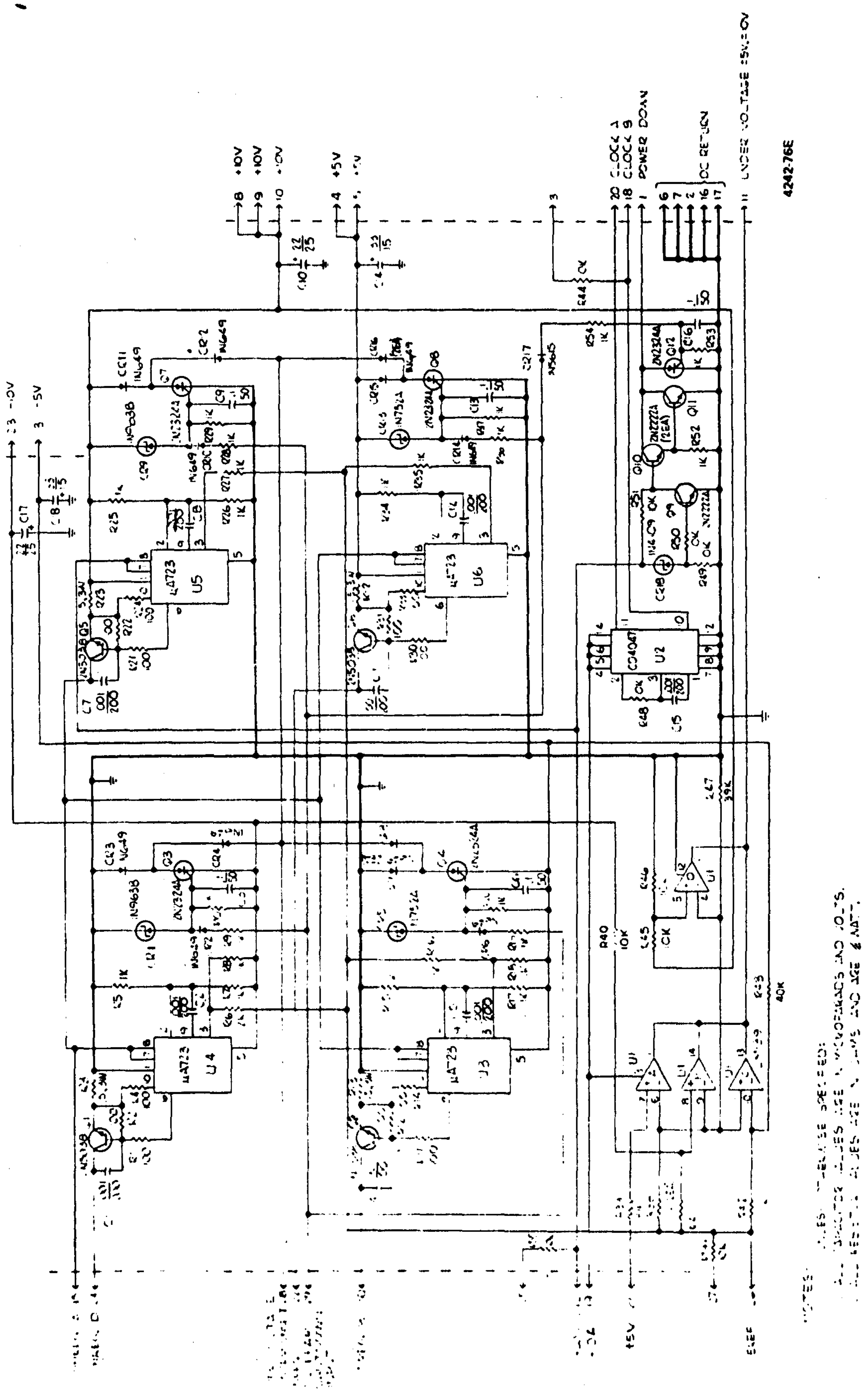


Figure 3-31. Power Supply, Module "A"

3.3.8.3.4.4 Module "H"

This card, see Figure 3-32 is a flyback converter for generating +55V to power the DSVT's and the operational description is synonymous with module "B", Section 3.3.8.3.4.2. The auxiliary overvoltage and start circuitry are unnecessary since the remainder of the supply accomplishes these functions indirectly on other cards. This module does make provisions for adjustable output and the overvoltage sense point because of the close tolerances involved.

3.3.9 Human Factors Engineering

The LGM design incorporates the requirements of MIL-STD-1472B to the maximum extent possible, consistent with operational requirements and physical design limitations imposed by TT-B1-2202-0013 performance specification.

Initial setup controls required to configure the equipment to system requirements are incorporated onto the accessible edge of the PCB's. These controls are protected by the front panel cover. The unit BITE control and alarm are positioned for rapid recognition and ease of identification.

Connections will be located on the rear of the case and are positioned to ensure maximum accessibility.

Unit weights imposed by the specifications are within the requirements of MIL-STD-1472B for lifting and carrying.

Refer to Section 15.4 of this volume for detail layouts of the LGM mechanical assembly.

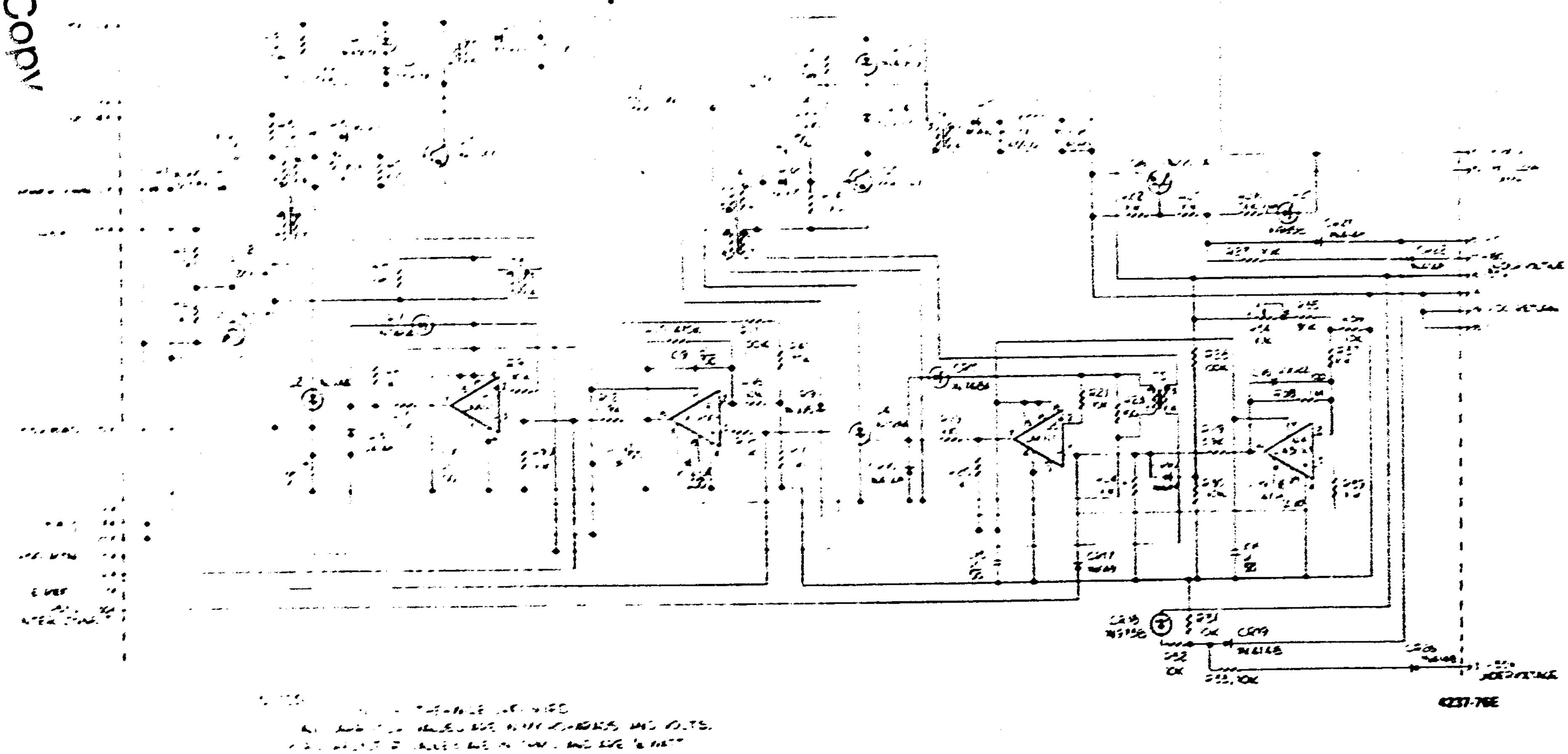


Figure 3-32. Power Supply, Module "H"

3.3.10 Reliability Design

The LGM has a specified MTBF of 3000 hours. This is equivalent to 333 failures in 10^6 hours. The reliability prediction and demonstrated results are summarized in Table 3-13.

TABLE 3-13

LGM RELIABILITY

Specified MTBF (Hrs)	Predicted MTBF (Hrs)	Demonstrated MTBF (Hrs)
3000	5057	13,100

3.3.11 Summary of PQT Results

3.3.11.1 Introduction

The LGM met or exceeded all major functional and evnironmental requirements. It is to be emphasized that the LGM has successfully passed all of the PQT tests, as well as all interoperability tests and the out-of-spec conditions found during testing are all of a minor nature and do not affect interoperability. The out-of-spec characteristics are summarized below:

a. Loop DSVT power feed: one sample only due to current starving of power supply 55 Vdc output.

b. Loop output impedance: too high due to high copper losses in coupling transformer.

c. Group Output Interface: rise and fall times, slew rates and unloaded offset were slightly out of spec due to the line driver type used.

d. Telemetry Output Offset: out-of-spec for the same reason as c. above.

e. Group Input and Station Clock input capacitance above spec: filter pins in I/O connectors were far above nominal capacitance value.

3.3.11.2 Problems/Solutions

The problems encountered during the testing of the LGM were not major and do not affect the mission of the equipment. Some of the problems, such as the Loop Modem output impedance, are common to the RLGM and RMC. Most of the problems are at the interfaces where the LGM interoperates with other equipment. Although the units interoperate properly, the interface specifications are not all met. Many specifications are too conservative and represent too pessimistic a view of the interface requirements for proper operation. The problems are presented below.

3.3.11.2.1 DSVT Power Feed

The output voltage requirement for the 55 volt output of the LGM power supply (Paragraph 10.10.3, steps 26 and 27, of CDRL Seq. No. F001) is 55V $\pm$ 2.5V to guarantee a DSVT power feed of 50V to 56V. The power supply 55 volt output of one LGM (Serial No. 014), when operating on low input voltage (103.5 Vac) at 420 Hz measured 51.6 volts. This caused the DSVT power feed to drop to 49.4 volts.

This failure is caused by the variation in the magnetics between power supplies. There is no need to increase the output of the power supply at this time. It is necessary to supply 48 volts at the loop output of the LGM for proper operation of the DSVT considering worst case wire and maximum power to the DSVT per Specification TT-A3-9002-0017A. The voltage is low only under full load and it is unrealistic to assume that all 16 DSVT's will be in use at the same time; the DSVT's actually require 1.3 watts, not the 2 watts used for testing. For this contract a waiver has been requested (Waiver No. 030 - DSVT Power Feed) to allow this particular supply to be used in the system.

For a future contract, tighter requirements at a higher output current would be placed on the power supply manufacturer.

3.3.11.2.2 Loop Channel Output Impedance

The requirement for loop channel output impedance (Paragraph 10.12.3, Step 2 of F001) is 125 ohms ±15% at 8, 16, 32 and 56 KHz. This requirement is also in the DGM Family Interface Control Drawing 910669, Paragraph 1.4.1b.

The impedance measured between 143.3 ohms and 167.9 ohms. The impedance is out of tolerance due to copper losses in the output coupling transformer and can be corrected by changing one series output resistor per loop channel (R38 and R50) from 120 to 91 ohms. This change would bring the impedance in specification.

There is no need to change the loop output impedance at this time as it does not impair the ability to use the DSVT. The multiplexer (LGM) operates error free for all cases of cable length and frequency with the DSVT. Operation with loops in excess of 6 KM was achieved; the specification is 3.2 KM.

For this contract a waiver has been requested (Waiver No. 029 - Loop Channel Output Impedance) due to the large quantity of printed circuit boards (413) that would have to be changed and the extensive retesting that would have to be done. The change would be incorporated in a subsequent contract.

3.3.11.2.3 Group Output Interface - Rise and Fall Time

Paragraph 10.21, Step 5 of electrical characteristics testing F001 and Paragraph 1.1.1.3 of the DGM Family Interface Control Drawing 910669 requires that the balanced output for the group data and timing signals of the LGM have rise and fall times no greater than 300 ns. The values measured as part of electrical characteristic tests ranged from 320 to 380 ns. The rise and fall time is limited entirely by the output driver and because the driver is current limited the output amplitude can be reduced by placing 620 ohm resistors from each output line to ground. With the decreased amplitude, the rise and fall times would be within the limits of the specification.

With the current design, the LGM has been shown to operate properly with all the interfacing equipment at this time, including the TED and the TRC-170. For this contract, a waiver has been requested (Waiver No. 034 - Balanced Output Rise and Fall Times). It would be very difficult to add the resistors to

the current design (a new PCB layout and a new build cycle for 44 cards would be needed). For a production contract, the resistors would be designed into the printed circuit card or a possible change to a faster line driver type would be considered.

3.3.11.2.4 Group Output Interface - DC Offset Voltage

Paragraph 10.21, Step 8 of electrical characteristics testing F001 and Paragraph 1.1.5 of the DGM Family Interface Control Drawing 910669 requires that the magnitude of the generator offset voltage measured from the center of a 100 ohm load to ground be no greater than 3 volts. The offset voltage measured as high as 4.8 volts for the group clock and data output of the multiplexer (LGM). This offset is caused by an imbalance in the line driver's ability to sink and source current. The solution is to add 620 ohm resistors to each driver output line to ground. With the resistors added, the dc offset would be within the limits of the specification.

There is no need to change the output of the LGM because all current interfaces are center tapped terminations to ground, eliminating the offset. This includes all the DGM equipment, the TED and the TRC-170. For this contract a waiver has been requested (Waiver No. 031 - Balanced Group Output dc Offset Voltage). It would be very difficult to add the resistors to the current design (a new PCB layout and a new build cycle for 44 cards would be needed). For a production contract the resistors would be designed into the printed circuit card or a possible change to another line driver type would be considered.

3.3.11.2.5 Group Output Interface-Slew Rate

Paragraph 10.21, Step 11 of electrical characteristic testing F001 and Paragraph 1.1.1.8 of the DGM Family Interface Control Drawing 910669 requires that the balanced output transition time of the LGM on the group data and timing signals between ± 40 mV shall be no more than 10 ns. The LGM's tested measured between 11 and 17 ns. This slew rate is limited entirely by the balanced line driver. These balanced drivers are located on the Interface printed circuit card.

For this contract a waiver has been requested (Waiver No. 033 - Balanced Output Slew Rate) because extensive testing of the LGM with the TED, the TRC-170 and equipment within the DGM family has proven that there is no problem interfacing with the current design. In future production, the only way to improve the slew rate would be to change the output driver type. It still may be necessary with a new driver to remove the filter pins from the interface connector creating a possible EMI problem. Another alternative would be a respecification to the current design to allow the slower slew rate.

3.3.11.2.6 Telemetry Output dc Offset Voltage

Paragraph 10.25, Step 7, of the electrical characteristic testing F001 and Paragraph 1.1.5 of the DGM Family Interface Control Drawing 910669 requires that the magnitude of the generator offset voltage measured from the center of a 100 ohm load to ground be no greater than 3 volts. The offset voltage measured as great as 4.8 volts for the telemetry output of the LGM. This offset is caused by an imbalance in the line driver's ability to sink and source current. The solution is to add 620 ohm resistors to each output line of the driver to ground.

For this contract a waiver has been requested (Waiver No. 035 - Telemetry Output dc Offset Voltage). At present there are no designated interfaces for the telemetry output, and interoperability is not affected. The drive circuits will work properly into a center tapped load to ground and will work into a non-center tapped load depending on the line receiver used in the interface. It would be difficult to add the necessary resistors to the timing generator card as it is now (a new layout would be required). In a future contract, the specification could be met by designing the resistors into the printed circuit card.

3.3.11.2.7 Group Input and Station Clock Input Capacitance

Paragraph 10.22 Group Input Interface Test and Paragraph 10.28 Station Clock Interface Test of electrcial characteristics testing F001 and Paragraph 1.1.2.2 of the DGM Interface Control Drawing 910669 require that the maximum input capacitance line to ground be no more than 3000 pf for the group clock, data and station clock inputs. The values measured as part of electrical characteristics test of the LGM measured from 3544 pf to 4149 pf.

The input capacitance is set almost entirely by the filter pins located in the interface connectors (J3 and J5), a small amount of capacitance contributed by wiring and circuit board etch. The filter pins used in the interface connectors are manufactured by Amphenol, Part No. 482-22 and are a Pi structure as shown in Figure 3-33.

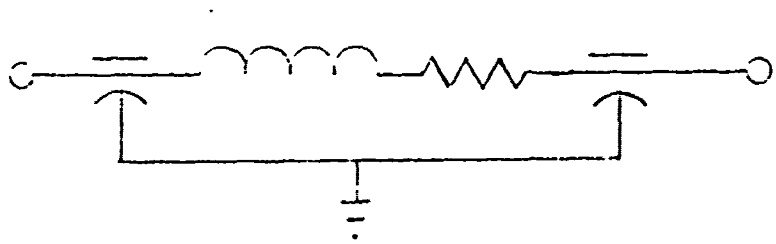


Figure 3-33. Filter Pin-Amphenol 482-22

Amphenol specifies that the minimum capacitance is no less than 2500 pf and that the cut-off frequency of the filter is no less than 3 MHz; nowhere do they specify the maximum value of the capacitance nor the value of the series resistor from which could be calculated the capacitance using the cut-off frequency. Because the capacitors are a coaxial structure it was assumed that the capacitance would be within 20% of the specified value or 3000 ph maximum; however, the filter pins measure as high as 4149 pf.

Extensive interface testing of the LGM with the TED, TRC-170 and equipment within the DGM family has proven that there is no interoperability problem with the current design. In a future production contract, the filter pin could be changed to a pin of lesser capacitance creating a possible problem with EMI. Another alternative would be a respecification to the current design to allow the use of the higher capacitance filter pin.

SECTION 5
RLGM

The Remote Loop Ground Multiplexer (RLGM) is used in tactical communications field locations (exposed) and also in shelters and vans. Its primary function is the time-division multiplexing of digital channels (loops) into a group, and the time-division demultiplexing of a loop group into its individual channels. Also provided by the design are a self-contained BITE capability for O&M support.

The Loop Modems contained in the RLGM transmits and receives 32 kb/s (or 16 kb/s) conditioned diphase signals on the cable connecting it to a DSVT and time division multiplexes these signals into a bit interleaved digital group signal. Inversely, group signals received on the RLGM's group side are demultiplexed into their constituent channels or loops which are sent to the DSVTs via the Loop Modems. The RLGM generates the overhead channel (one-half rate) which provides framing and SYSCON telemetry information. The group framing and synchronization element generates and detects the frame synchronization patterns required to maintain link synchronization. Frame sync acquisition is initiated when the out of sync condition is detected. The Group Modem element transmits and receives the NRZ group signal from the multiplex-demultiplex element and transmits and receives conditioned diphase group signals from the cable connecting the RLGM to an interfacing DGM equipment.

Internal timing signals required by the RLGM elements are generated by the clock and timing generator element. This element operates on external station clock signal or recovered timing from the RLGM Group Modem element. The BITE element monitors RLGM performance and provides fault detection and isolation. RLGM DC power is obtained from the power supply element which operates from AC or DC primary sources. This element also provides power to the RLGMs interfacing DSVTs for common battery operation. Alternately, the RLGM and its DSVTs can have power fed to them from an interfacing

RLGM CD or an RMC on its group side. An analog voice orderwire is provided for set up and maintenance of cable systems utilizing CX-11230 cable.

Physically, the RLGM design and construction provide a rugged, compact and modularized equipment package.

5.1 DESIGN GOALS AND REQUIREMENTS

The RLGM functions are summarized in Table 5-1.

The major design objectives in the RLGM were directed toward reducing the weight of the unit. To this end, C-MOS devices were used throughout its design. These devices accrue a substantial power savings over low power Schottky devices, permitting the use of smaller and lighter power supplies. However, the RLGM is used in exposed field units necessitating the use of first and second level protection devices as well as reinforcing structural elements to insure survivability during the drop tests. Because of these requirements there was very little flexibility or alternatives which could be applied in minimizing the unit weight. The unit weight is now 16.9 KG.

TABLE 5-1. FUNCTIONAL REQUIREMENTS - REMOTE LOOP MULTIPLEXER (RLGM)

Definition: The remote loop side multiplexer shall multiplex 4 loop channels into a digital time division multiplexed loop group.

	Loop Side	Group Side
Type of Channels:	4 wire full duplex	Same
Number of Channels:	4	4.5
Bit Rate:	32/16 kb/s	144/72 kb/s
Modulation:	Conditioned Diphase	Conditioned Diphase
Used With:	DSVT	RMC/CNCE/TGM/RLGM/CD
Cable Type:	WF-16 Field Wire	CX-11230
Distance:	160 meters	3.2 KM
Power Feed:	DSVT per TT-A3-9002-0017	
Impedance:	125Ω ± 10%. Return loss ≥26 dB in the band from 8 to 56 kHz	
Orderwire:		Analog Voice (maintenance)
Termination:	4 Binding Posts for each loop	UG-1837/U
Timing:	External station clock 72/144 kb/s or derived from the received group signal. Loss of received group signal for 0.5 seconds shall not cause loss of BCI	
Overhead Channel Structure:	4 subchannels, one channel is framing, a second is telemetry	
Modularity:	4	4.5 (0.5 rate overhead channel)
Size:	8.5" H x 13" D x 17.5" (without transit covers) may be rack mountable by adding bracketry supplied by government	
Input Power:	60 watts maximum	

TABLE 5-1. FUNCTIONAL REQUIREMENTS - REMOTE LOOP MULTIPLEXER (RLGM) (Cont.)

	Loop Side	Group Side
Type of Power:	115 VAC $\pm$ 10%, 50 to 400 Hz or +28 VDC $^{+4}_{-6}$ volts or remote feed from an RMC or RLGM/CD	
Weight:	15.5 KG maximum (without transit covers)	
BITE:	Power Monitor/Fault Isolation	
Reliability:	4000 Hours MTBF	

5.2 DESIGN APPROACH

5.2.1 Summary

There are a number of basic design approaches which the subcontractor used throughout the design of the RLGM to optimize commonality with the Raytheon units. Basic design approaches were as follows:

a. The extensive use of C-MOS devices (refer to section 3.2.1)

b. The use of common printed circuit boards between the field and shelter units

c. Minimized the design of the loop modem circuit so that two loop modem's were packaged on a single P.C.B.

d. Designed the power supply so that common circuit designs are used in the field and shelter units

e. Designed the loop modem P.C.B's so that they are completely interchangeable with the loop modem P.C.B's used in the shelter units

f. Designed a Clock and Timing P.C.B. which may be interchangeable with the Clcok and Timing P.C.B's located in the LGM and RMC units

g. Designed the Group Modem P.C.B. so that it may be interchangeable with other Group Modem P.C.B's located in the LGM and RMC units.

h. Other mechanical design approaches are discussed in paragraph 15.4 of this volume.

5.2.2 Detailed Electrical Design of the RLGM

A detailed block diagram of the RLGM is shown in Figure 5-1. The RLGM multiplexes 4 1/2 channels into a digital time division multiplexed loop group. The half rate channel is the overhead channel which transmits framing and telemetry data. The RLGM contains four (4) conditioned diphase loop modems. Two modems are packaged on a single P.C.B.

The loop modems accept baseband digital loop signals from the MUX/DEMUX P.C.B. and modulate/demodulate the loop data for transmission to digital voice subscriber terminals via telephone (WF-16) cable. The modems also provide phantom loop power over this same cable to power the DSVT operating in a common battery mode. A switch is provided on each loop modem to control the power (on/off) to each DSVT. EMP devices required for first level protection are mounted on the RLGM's signal entry panel for each loop. Second level EMP protection circuits are located on each loop modem.

The Loop Modems NRZ baseband data is passed to the MUX/DEMUX card where it is multiplexed with the overhead channel containing the SYSCON sub-channel. The resulting bit interlaced data stream is sent to the Group Framing Unit where the data is gated to the output group data interface under control of the synchronizer section of the Group Framing Unit. The output group baseband data stream is connected to the Group Modem. The Group Modem converts the baseband data to conditioned diphase for transmission on the RLGM group output.

The input group data is demodulated by the Group Modem producing a baseband signal compatible with C-MOS logic. The Group Modem also performs the clock recovery function which is required to lock the RLGM's internal Timing Generator to the incoming data stream when station clock is not used.

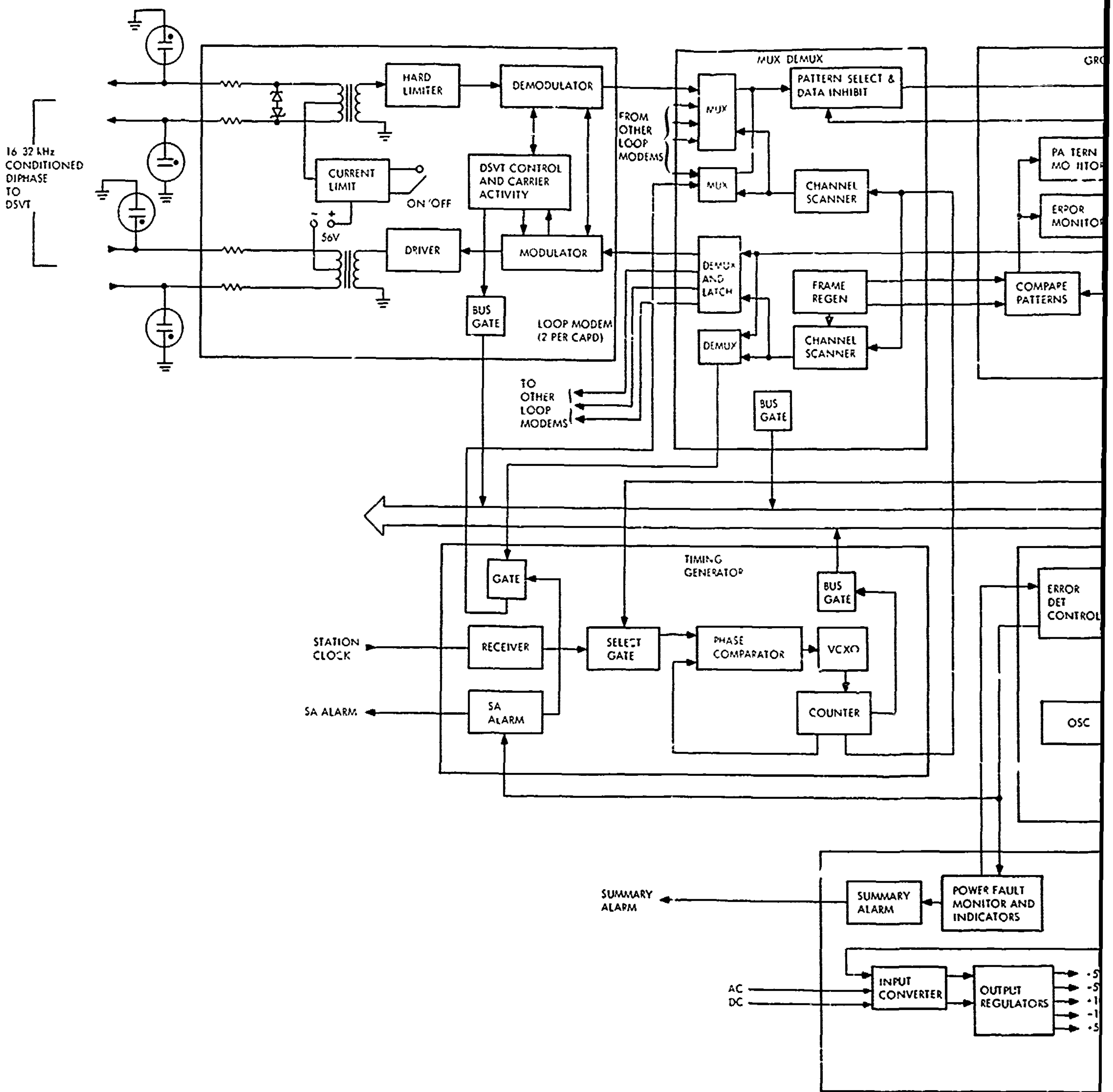
The baseband data is then connected to the frame regenerator portion of the Group Framing Unit. The frame regenerator is a counter whose output (frame pattern) is aligned in phase with the incoming frame pattern in the data. The frame reference is used to properly phase the MUX/DEMUX circuitry. The demultiplexed data channels are buffered, and applied to each loop via the Loop Modems. Binding post terminals, mounted on the RLGM's signal entry panel, are used to connect each loop with the DSVT's.

An analog voice orderwire channel is provided for set up and maintenance of cable systems utilizing CX-11230 Cable. The appropriate filters required to separate the orderwire analog signal from the data are located on the Group Modem. An external connector is provided on the RLGM's signal entry panel for connection to the Cable Orderwire Unit (COU).

The Timing Generator locks an internal oscillator to either an external clock or to the incoming groups recovered clock. A toggle switch located on the Group Modem P.C.B. is used to select this function. Toggle switches located on the Timing Generator P.C.B. are used to program the proper output clock rates, the switch outputs are also used to program the MUX/DEMUX card.

Capability of looping back the SYSCON subchannel is provided on the Timing Generator P.C.B. The loop-back function is interrupted and all ZERO's are inserted at the input to the sub-channel multiplexer when a Summary BITE error (SA) has been detected.

The BITE card monitors key signal status on each P.C.B. within the RLGM. These signals are transmitted to the BITE P.C.B. over a sixteen (16) bit buss. The BITE P.C.B. sequentially addresses each P.C.B. within the unit and determines whether all the "key" signals are present. If not, a one second delay is started and the signals tested again. If after the one second delay, the fault persists, a summary error flag is raised. This flag causes the S and the SA (depending upon the fault) alarm's to be energized.



16 32 kHz CONDITIONED DIPHASE TO DSVT
HARD LIMITER
DEMODULATOR
CURRENT LIMIT
ON/OFF
56V
DSVT CONTROL AND CARRIER ACTIVITY
DRIVER
MODULATOR
BUS GATE
LOOP MODEM (2 PER CAPD)
MUX DEMUX
MUX
PATTERN SELECT & DATA INHIBIT
FROM OTHER LOOP MODEMS
CHANNEL SCANNER
DEMUX AND LATCH
FRAME REGEN
DEMUX
TO OTHER LOOP MODEMS
BUS GATE
COMPARE PATTERNS
ERROR MONITOR
TIMING GENERATOR
GATE
STATION CLOCK
RECEIVER
SELECT GATE
PHASE COMPARATOR
VCXO
COUNTER
SA ALARM
ERROR DET CONTROL
OSC
SUMMARY ALARM
POWER FAULT MONITOR AND INDICATORS
AC
DC
INPUT CONVERTER
OUTPUT REGULATORS

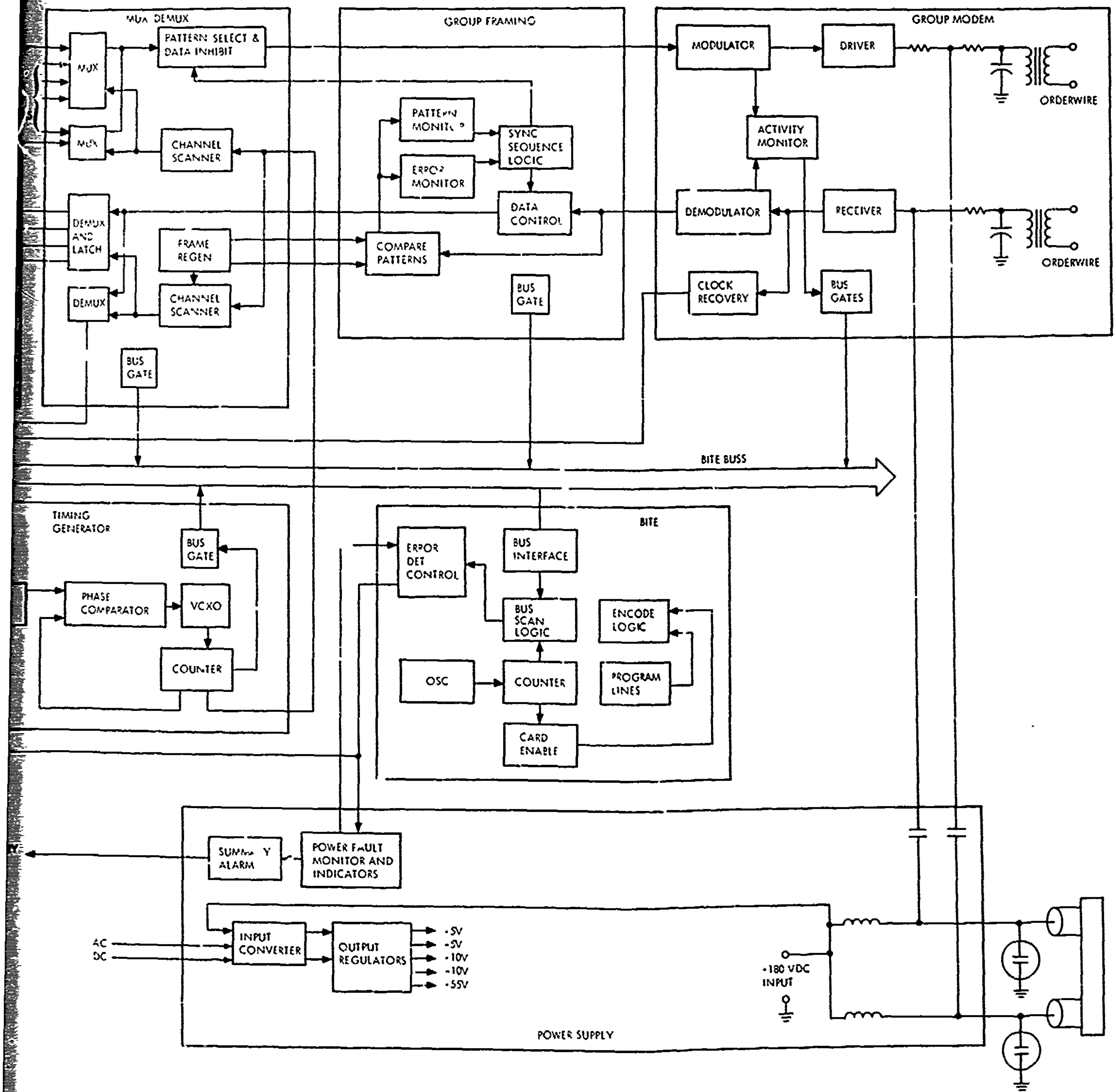


Figure 5-1. RLGM Block Diagram

2

An LED located on the defective P.C.B. is then illuminated along with the Summary Error indicator located on the front panel of the power supply. In the event that the BITE has detected, a fault which could be caused by an external error (interface unit), the LED located on the BITE P.C.B. will illuminate. The fault LED located on the BITE P.C.B. is used to indicate external errors only.

The RLGM power supply operates from +28 VDC, 120 Volt AC, 50 to 400 Hz single phase power or remotely from a +180 VDC power source. The 180 VDC is supplied to the RLGM over the CX-11230 cable from either an RLGM/CD or RMC. The de-coupling capacitors and chokes which are used to separate the DC power from the cable are located in the power supply.

The power supply outputs are ± 10 VDC, +5 VDC, and +55 VDC. The 5 and 10 VDC voltages are used internally to power the RLGM P.C.B.'s. The +55 Volt output is used for powering the DSVT's via phantom loops. The Power Supply contains fault monitoring circuits which monitor the status of each output voltage. When an out-of-tolerance indication is detected, the Power-out-of Tolerance and Summary Fault indicators are illuminated.

5.2.3 Interface Description

The Remote Loop Group Multiplexer (RLGM) is a standalone unit designed for field-portable, exposed use. The width of the RLGM case is small enough to allow mounting to MIL-STD-189 racks within a shelter or van. Appropriate mounting brackets (not supplied) are required for this type of installation.

The RLGM can multiplex up to four digital subscriber loops with an overhead channel into a single output digital time division multiplexed loop group. The loop group consists of a 4 1/2 channel group. The overhead channel operates at one-half the rate of the input subscriber loops. The overhead channel is used to transmit framing and telemetry data.

The RLGM interface requirements are summarized in Table 5-2 and are described in the following sections.

5.2.3.1 Loop Interface (16 Binding Posts)

The RLGM loop interfaces are provided to connect to 4 full duplex digital loops. Each loop interface consists of transmit loop data and receive loop data. The signals are conditioned diphase. The line is balanced. The signal rates are 16 kb/s or 32 kb/s. The power feed to each DSVT is provided on each line through a phantom loop. This voltage is fifty-five volts maximum (measured at the RLGM terminals). A maximum of two watts per DSVT can be supplied by the RLGM. Connections to the DSVTs on the loop side are by WF-16 field wire. Sieman's gas-filled surge arrestors are used as first level EMP protection. One arrestor is placed across each binding post terminal. The binding post is permanently mounted to the Signal Entry Panel (SEP) of the case. The connections from the SEP binding posts to the P. C. B. nest are by direct wiring. Refer to the RLGM mechanical layout in Section 15.4.2 of this volume.

5.2.3.2 Group Interface (J1)

The RLGM input group interface interfaces with a full duplex digital group which connects to a Group Modem (GM). The input group interface consists of transmit group data and receive group data. The signals are conditioned diphase. The line is unbalanced. The signal bit rates are 72 kb/s when the loop is 16 kb/s and 144 kb/s when the loop is 32 kb/s. DC power is supplied by a Remote Multiplexer combiner or an RLGM Cable Driver to power the RLGM remotely. The RLGM also has provisions to power the unit from a self-contained power supply. Connections to the Group Interface are by CX-11230 coax cable; remote power to the RLGM is supplied over this cable.

TABLE 5-2. RLGM INTERFACE SPECIFICATION SUMMARY

Connector	Function	Signal Rate/ Frequency	Signal/Line Characteristics	Type of Cable Connection Required	Number of Wires in Connector
16 Binding	• Transmit and Receive Loop Data - Channels 1 through 4	16 or 32 kb/s	Conditioned Diphase, Balanced	8 TP (Field Wire-WF-16)	---
J1	• Transmit Group Data • Receive Group Data	72 kb/s or 144 kb/s for loop rates of 16 or 32 kb/s respectively	Conditioned Diphase, Unbalanced	UG-1837 (Dual Coax)	2 Coax
J2	• Station Clock	72 kb/s or 144 kb/s	NRZ, Balanced	1 shielded twisted pair	3
J3	• SA Alarm • Alarm (Output)	Contact Closure Contact Closure	---	2 twisted pair with overall shield	5
J4	• Prime Power	AC 50, 60, or 400 Hz or DC +28 volts	---	3 conductors	3
J5	• Orderwire In • Orderwire Out	300-3500 Hz Analog	600Ω Balanced	2 twisted pair with overall shield	5

5.2.3.3 External Clock Interface (J2)

The clock signal is at the group rate of 72 or 144 kb/s. The line is balanced.

5.2.3.4 ALARM Signals (J3)

A common connector is provided to carry a contact closure for the SA ALARM and a contact closure for the S ALARM output.

5.2.3.5 ORDERWIRE (J5)

A full duplex voice frequency orderwire access is provided on J5. The signal is balanced, analog with a nominal bandwidth of 300 to 3500 Hz. Input impedance is 600 ohms, $\pm$ 10%.

5.2.3.6 Prime Power (J4)

A common connector is provided to accept the prime power to the RLGM. The input power is 115 VAC $\pm$ 10%, 50 to 400 Hz or +28 $\left({}^{+4}_{-6}\right)$ volts DC.

5.3 DETAIL ELECTRICAL DESIGN

5.3.1 Introduction

As was previously explained, logic elements were designed into P.C.B's which are used in more than one unit. This was possible since there are many functions which are similar in these units. Consequently, it was decided to design these cards with emphasis on commonality. Variations in specific unit functions are taken care of by either toggle switches mounted on the P.C.B. or by back-plane wiring. For purposes of this technical report, we will describe the card in detail in the first section covering that material. References will then be made to this paragraph in subsequent sections.

5.3.2 Loop Modem

The loop modem is a WF-16 field wire carrier terminal which provides full duplex transmission of binary data signals at 32/16 kb/s between DSVT terminals and the RLGM.

Figure 5-2 illustrates the block diagram of the diphase modulator. Refer to section 3.3.5.1 for the description.

Figure 5-3 illustrates the block diagram of the diphase demodulator. Refer to section 3.3.5.2 for the description.

5.3.3 MUX/DEMUX

The multiplexing and demultiplexing function in the RLGM is achieved by a common P.C.B. (refer to figure 3-4 for the block diagram of the MUX/DEMUX) which multiplexes 4 loop channels and 4 subchannels to make up a 4 1/2 channel output group as shown in Figures 5-4 and 5-5.

For detailed information on the MUX/DEMUX P.C.B. refer to section 3.3.2 of this volume.

The MUX/DEMUX card in the RLGM is fixed by back-plane wiring to provide the 4 1/2 channel Output Group format.

The multiplexer contains three eight (8) bit multiplexers, one for the four (4) loop inputs, one is unused, and one for the four (4) subchannels. The overhead channel generator divides the group bit clock by nine (9) establishing the proper position for the overhead channel and a pattern sequencer which enables the multiplexers in the proper sequence to produce the output pattern shown in Figure 5-4.

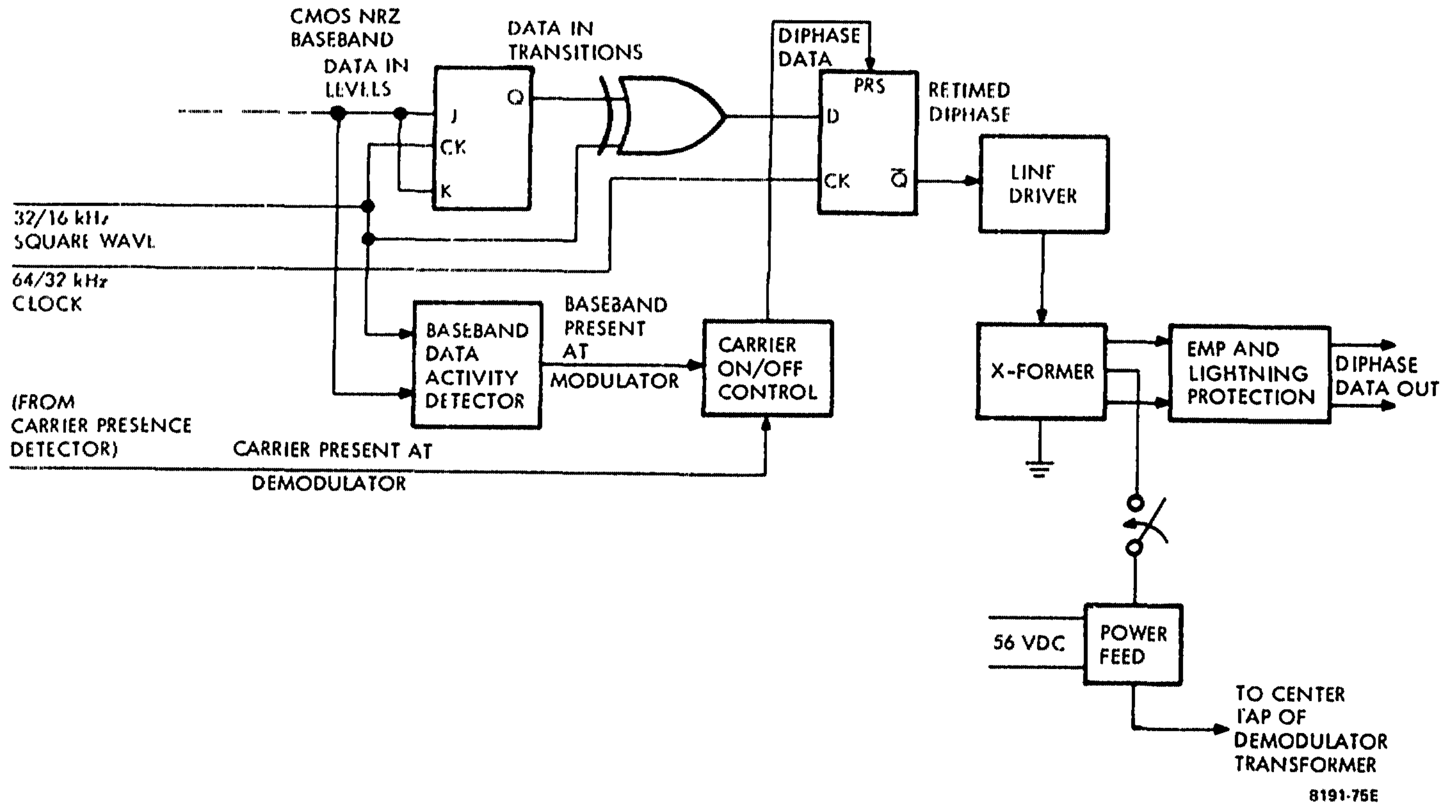


Figure 5-2. Loop Modem Modulator Section

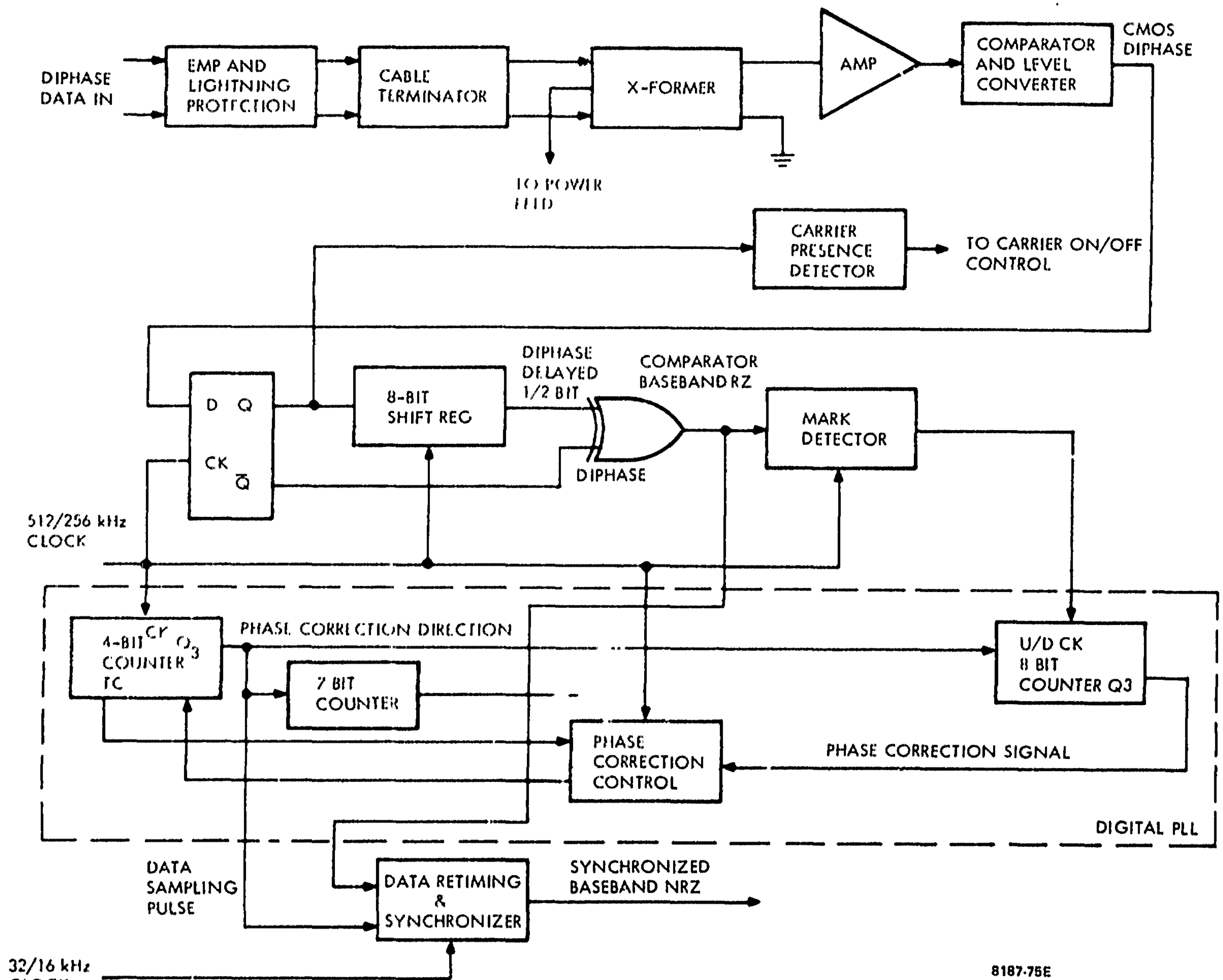


Figure 5-3. Loop Modem Demodulator Section

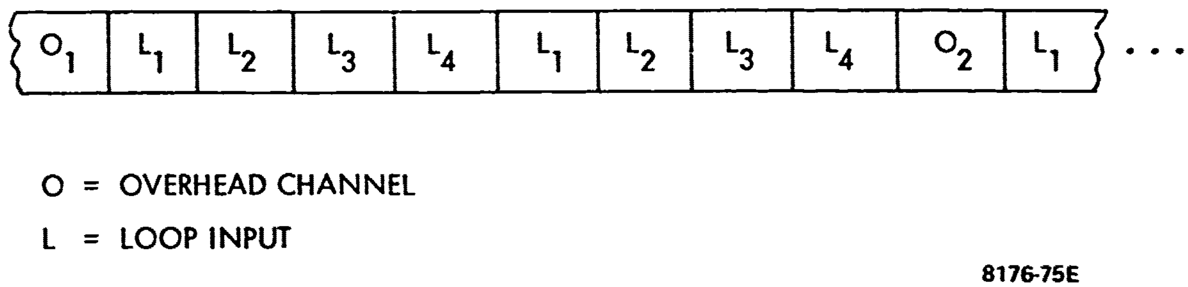


Figure 5-4. RLGM Output Format

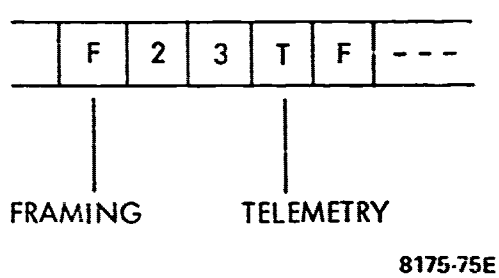


Figure 5-5. Overhead Channel Format

Multiplexer C, refer to section 3.3.2, multiplexes 4 subchannels together that make up the overhead channel. The 1st of these subchannels is for framing and will be alternating 1-0 or all 1's as selected by the frame pattern select circuitry. This frame pattern selection is determined by the pattern control signal from the synchronizer card. Channel 1 of the subchannels (subchannel just after the framing subchannel) is for SYSCON Telemetry which is looped back to the demux side through a gate whose state (open or closed) is controlled by the BITE.

The remaining subchannels are set to logic level "1".

The output control circuitry can inhibit the data channels from the mux upon command from the synchronizer card. The Data Control signal provides the control to either output normal data or all 0s in the data channel time slots. In either case, the frame pattern is passed through unaltered. The data is then passed through the Group Modem.

5.3.3.1 Demultiplexing

The channel demux receives reframed data and a frame reference from the framing card and demultiplexes the data into 4 loop channels and 4 overhead subchannels in a manner similar to the multiplexer. The 1st subchannel (subchannel just after the framing subchannel) is routed to an external output.

5.3.4 <u>RLGM: Framing/Synchronizer Unit</u>

The Framing/Synchronizer card used in the RLGM is identical to the card used in the LGM (see section 3.3.3) with the following exceptions: the RLGM does not provide a "squelch" input for inhibiting frame search and does not include provisions for a TED. The manual switch located on the card edge "TED equipped/non-equipped" is nonfunctional: the proper switch position is hardwired on the back plane.

A block diagram of the framing portion of the card is shown in Figure 5-6 and the synchronizer in Figure 5-7.

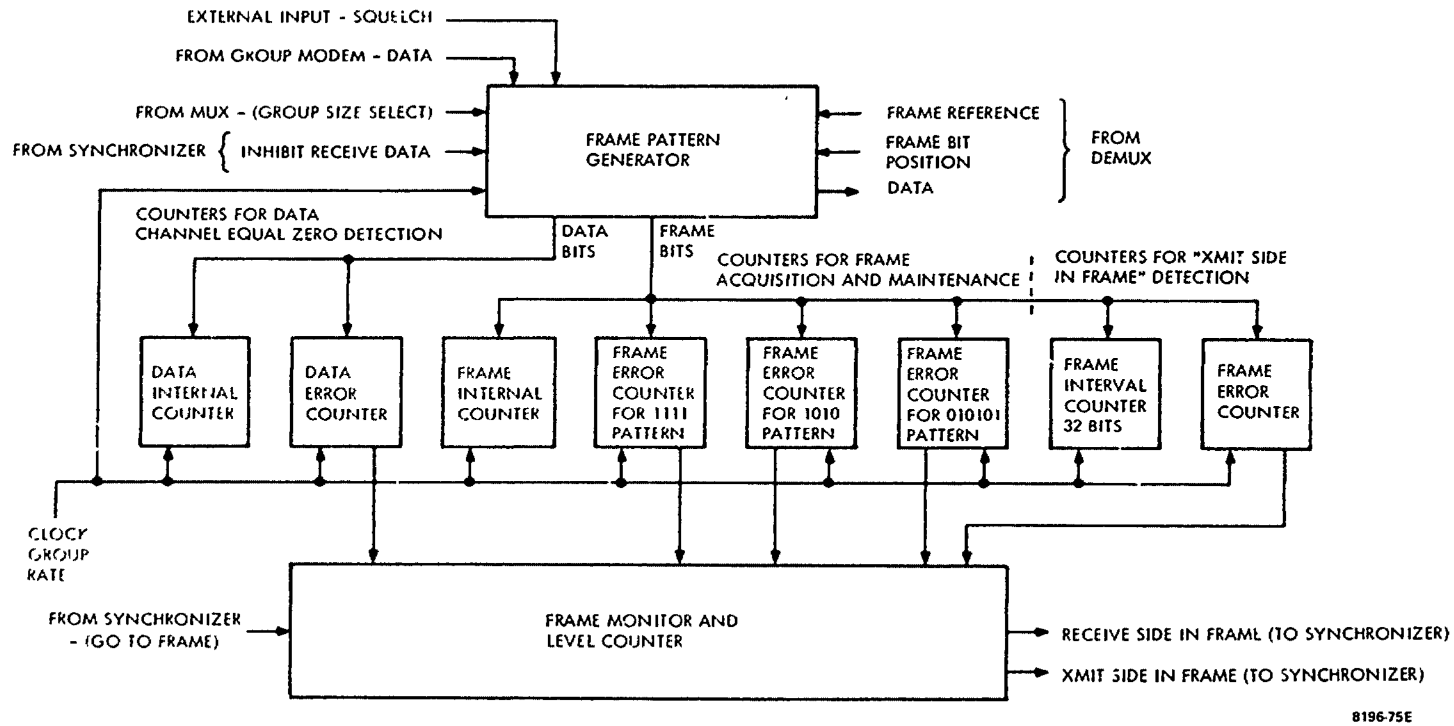


Figure 5-6. Framing Block Diagram

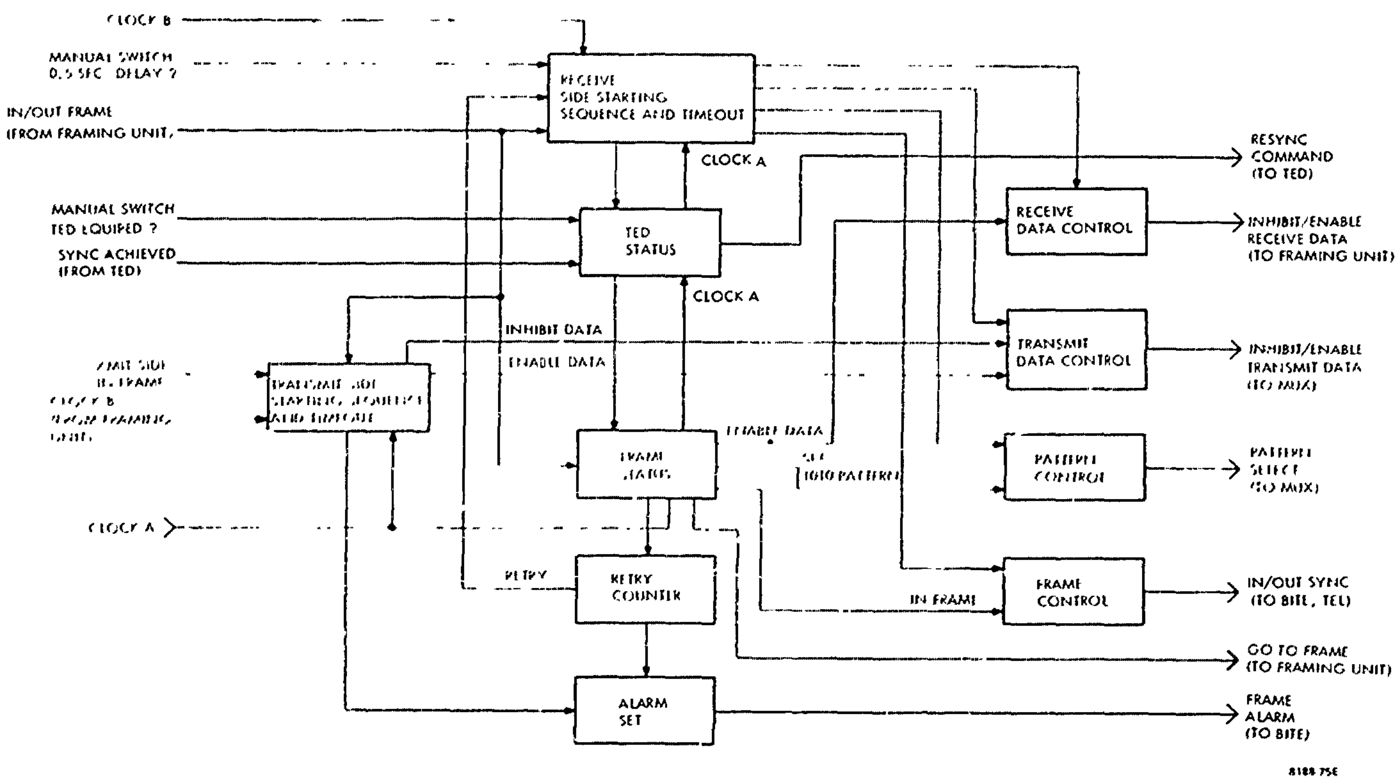


Figure 5-7. Frame Synchronizer Block Diagram

5.3.5 Group Modem - RLGM

The Group Modem (GM) provides full duplex transmission of synchronous binary data signals at the group level. The data is transmitted via conditioned diphase-modulated carrier over CX-11230( )/G coaxial cable.

5.3.5.1 Diphase Modulator

Figure 5-8 is a functional block diagram of the modulator section in the GM. The modulator accepts a binary baseband data stream and converts the baseband signal to a band-limited conditioned diphase modulation signal for transmission over coaxial cable. The following elements make up the modulator. The JK flip-flop samples of the baseband data with the group rate clock. When the data is a mark (one), the JK flip-flop toggles. The output of the JK flip-flop is conditioned baseband. A transition in the conditioned baseband represents a mark (one). The conditioned baseband is modulo two added to the bit rate clock (square wave). The resulting output is a conditioned diphase modulated version of the input baseband data. The diphase is retimed by the D flip-flop to remove glitches.

The line driver provides the drive current to couple the diphase modulated carrier into the coaxial line. The output signal level is 3V p-p $\pm$10%; the rise and fall times are nominally 5% of the bit period.

The carrier presence detector generates the Loss of Carrier alarm whenever the output carrier is not present.

5.3.5.2 Diphase Demodulator

Figure 5-9 is a block diagram of the demodulator. The GM demodulator accepts diphase-modulated signals from the cable and delivers a baseband data stream to the MUX/DEMUX. In the event of loss of carrier, the phase-lock loop corrections in the Timing Generator card are inhibited and the system runs off the clock phase selected prior to the outage. The recovered clock is

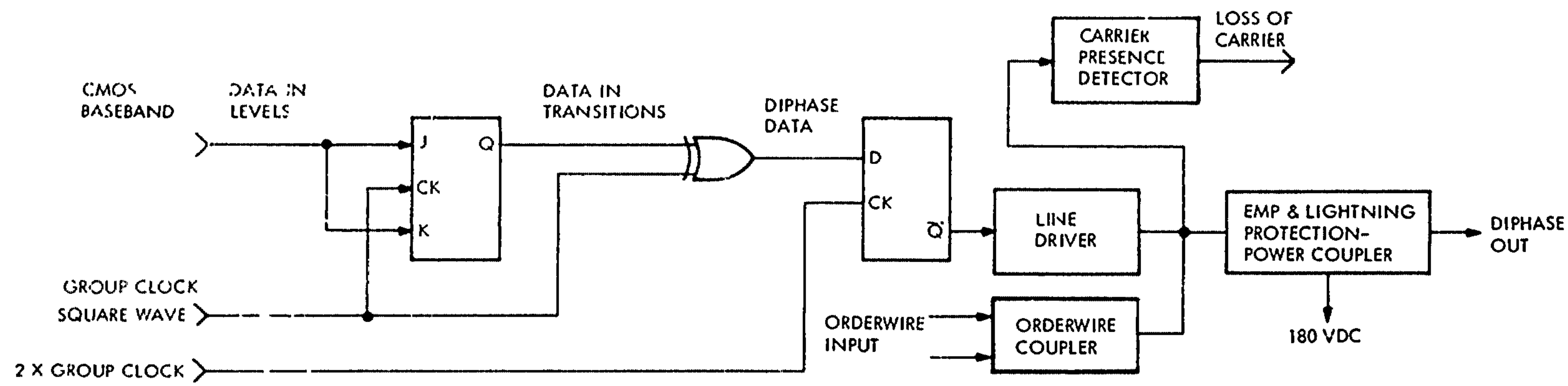


Figure 5-8. Group Modem Modulator Section

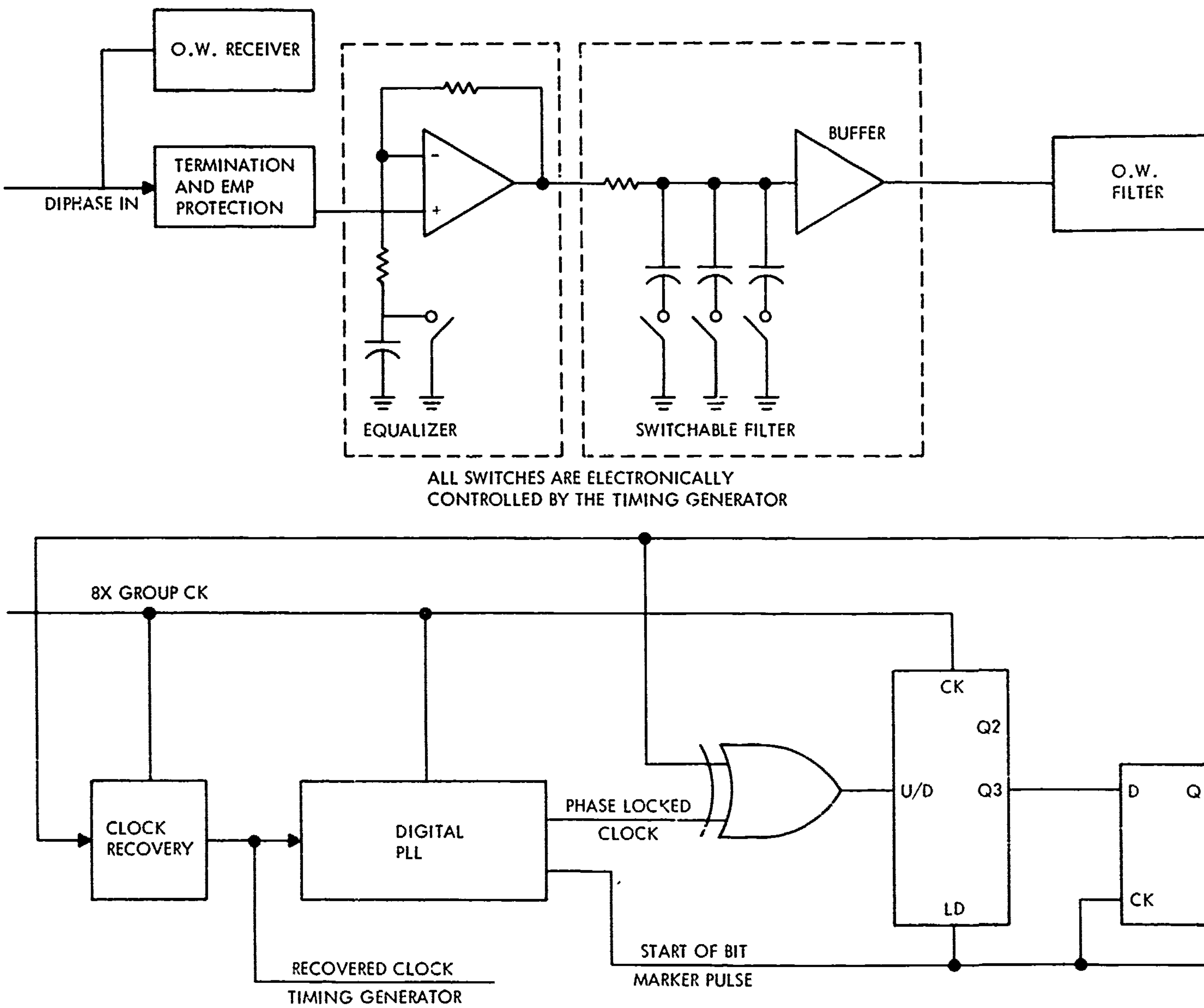
outputted to the Timing Generator unit. The receive signal level must be greater than 150 mv in order to be detected. A fixed equalizer is provided to compensate for the phase and amplitude distortion of up to 3.2 km of CX-11230( )/G cable. Over compensation for short lengths is clipped off in the limiter. The clock recovery circuit reconstructs a square wave bit rate clock from the received hard-limited diphase-modulated signal.

The input stage of the demodulator is automatically programmed to equalize and low pass filter the signal. The bit rate controls the low pass filter cutoff frequency and whether the equalizer is switched in or out.

The orderwire filter is a high pass filter with a cutoff of 7 kHz. Its function is to prevent the analog voice from causing excessive errors. The orderwire filter feeds the comparator, which hard limits the analog diphase, and the loss of signal detector, which supplies a signal to the PLL in the timing generator.

The clock recovery circuit is edge triggered by the hard limited diphase to produce a recovered clock at the bit rate. The recovered clock is used by the timing generator in the recovered clock mode. The recovered clock also feeds a digital PLL, which provides a stable group rate square wave with known phase relation to the diphase. The digital PLL is designed to track 47 ppm frequency jitter on the incoming diphase. The phase locked clock is phase compared with the diphase to produce phase transition data. The phase transition data, which contains glitches and disturbances caused by noise is integrated by the UP/DOWN counter to improve nose performance. The start of bit marker pulse causes the UP/DOWN counter to integrate and dump over the bit interval. Before the count is dumped, it is sampled by the D flip-flop. The output of this flop is clean phase transition data.

The second "D" flip-flop and the Exclusive OR gate convert the phase transition data to baseband NRZ. The FIFO accomplishes two things; first it


O.W. RECEIVER
TERMINATION AND EMP PROTECTION
DIPHASE IN
BUFFER
O.W. FILTER
EQUALIZER
SWITCHABLE FILTER
ALL SWITCHES ARE ELECTRONICALLY CONTROLLED BY THE TIMING GENERATOR
8X GROUP CK
CK
Q2
U/D
Q3
D
Q
CK
LD
CLOCK RECOVERY
DIGITAL PLL
PHASE LOCKED CLOCK
RECOVERED CLOCK
TIMING GENERATOR
START OF BIT MARKER PULSE

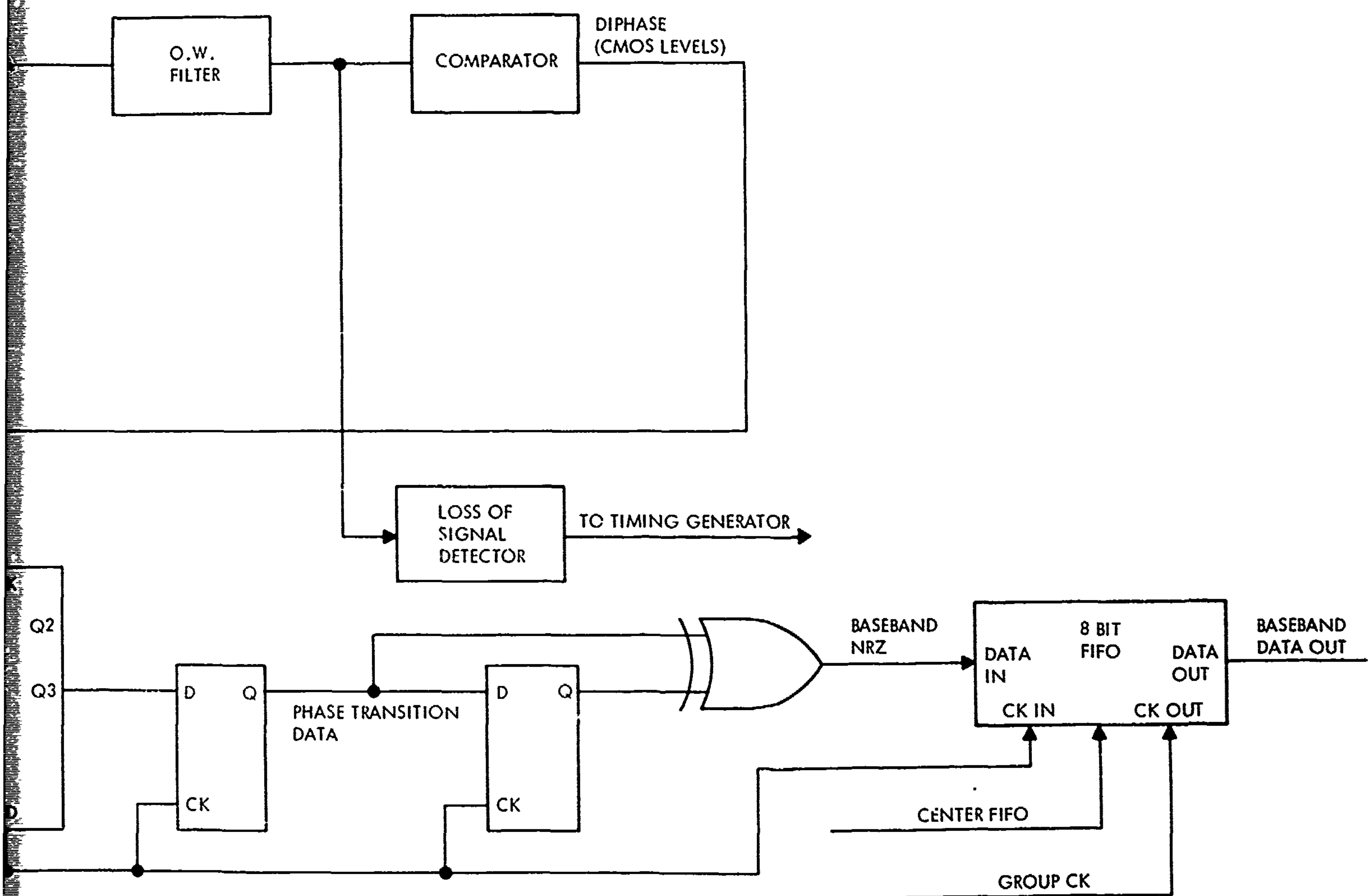


Figure 5-9. Group Modem Demodulator

2

synchronizes the data to the system group clock; secondly, it will absorb path length variations up to 8 bits. Each time the system goes out of frame, the FIFO is centered.

5.3.5.3 Power Feed

The RMC can supply power to the RLGM. The scheme is illustrated in Figure 5-10. The power is transmitted over the center conductors of the coax cable.

5.3.5.4 Orderwire

The RLGM and RMC provides a passive analog voice frequency orderwire circuit for use in the maintenance of the equipment. The circuit is passive and allows the COU to connect to the cable through a transformer and coupling circuit. The channel bandwidth is a nominal 300 Hz to 3500 Hz. The frequency limits and losses are shown in Figure 5-11.

The provision of power feed, orderwire and diphase traffic on the same cable are done with the circuits shown in Figure 5-10. In that figure a high pass filter follows the receiver amplifier. This filter is a two pole Butterworth filter whose 3 db cut-off is 7 kHz. The purpose of the filter is to remove voice from the traffic before it is demodulated. A single capacitor on the secondary of the orderwire transformer in Figure 5-10 filters the diphase out of the voice to some degree.

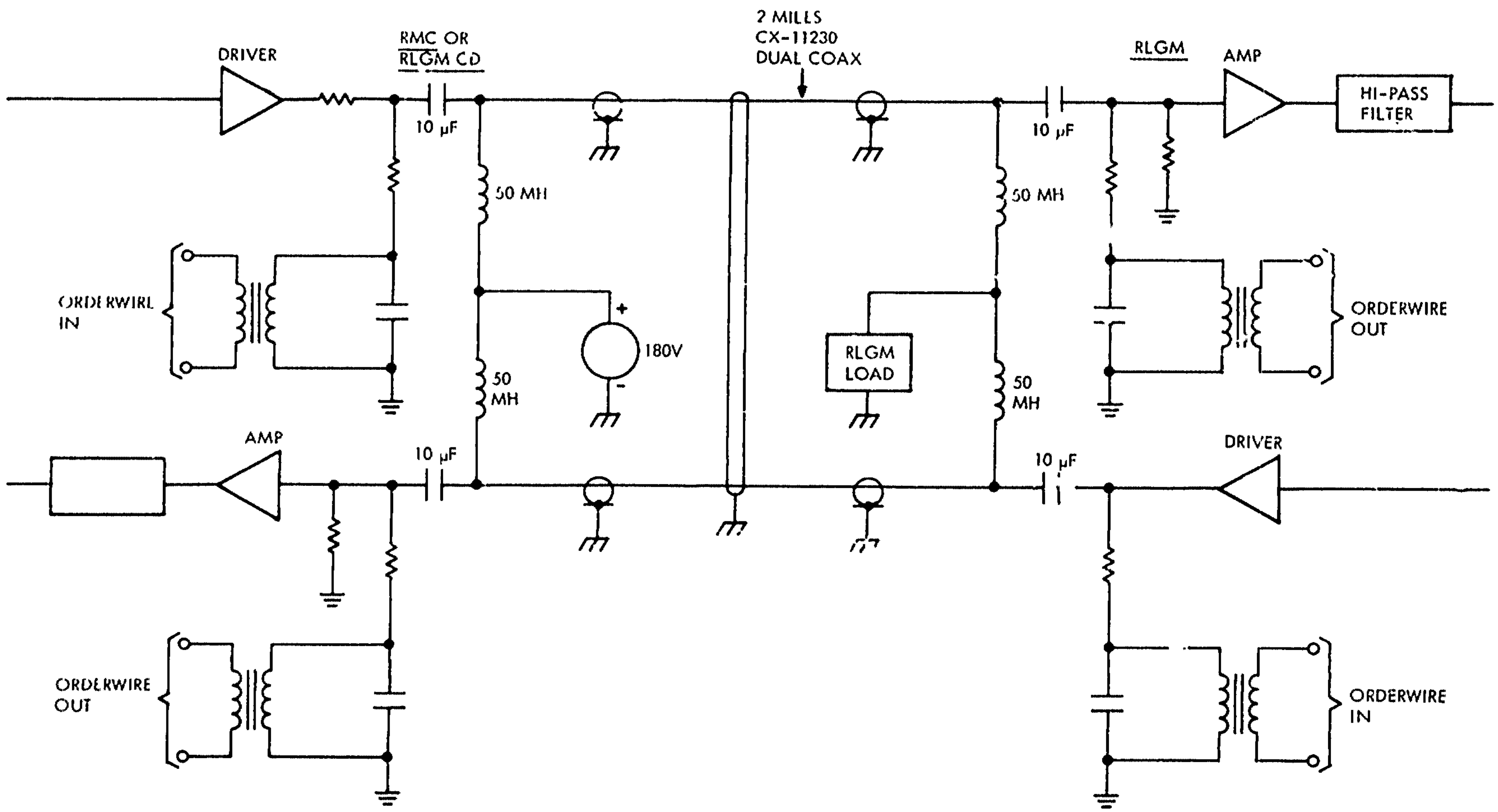


Figure 5-10. Power Feed and Orderwire Circuits for RLGM and RMC Group Modem

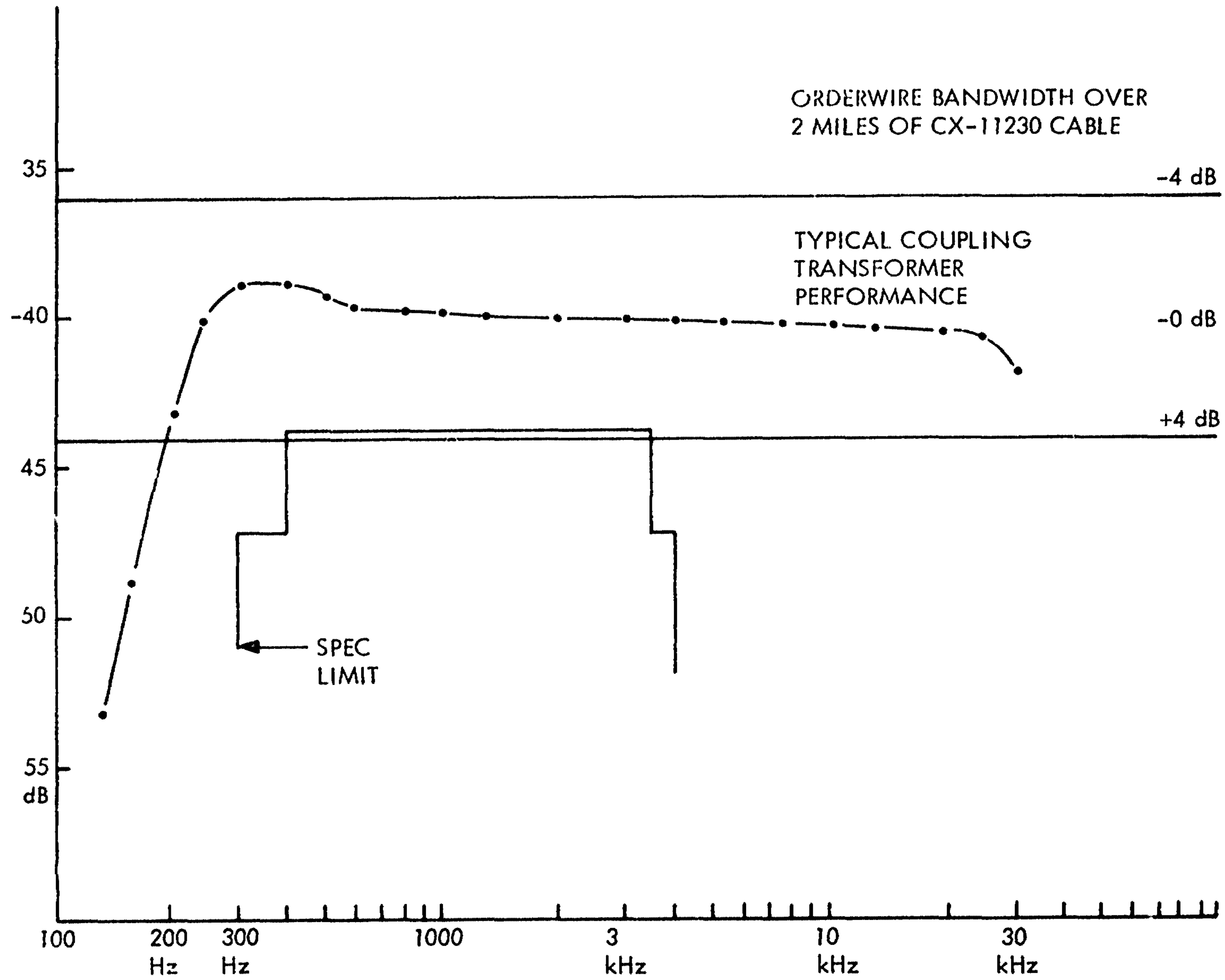


Figure 5-11. EOW Specification Limits

5.3.6 Timing for the RLGM

The same Timing Generator card is used in the LGM, RLGM, and RMC. Various combinations of rates are required in the different units; the rate combinations are shown in Table 5-3. A block diagram of the Timing Generator is shown in Figure 5-12. Rate select switches S1, S2 and S3 are disabled in the RLGM back plane wiring. A strap on the card selects the rate family based on 16 or 32 kb/s channel rates. Details of the clock and timing design are given in section 7.3.6 of this volume. Clock line outputs which are blank in the table are not wired in the RLGM back plane.

5.3.7 BITE

5.3.7.1 Introduction

Built-in test equipment (BITE) monitors signals in and out of the unit and internal circuits. Go-no-go fault location circuits isolate failures to a particular printed circuit card or least replaceable unit (LRU) (i.e., power supply). The BITE operates without interrupting traffic or interferring with normal system operation and removal of the BITE card does not affect operation of the LGM, RLGM or RMC. Failure alarms are provided on a card-by-card basis and operated with a time guard of one second. Two relays are used to generate contact closures when an alarm occurs. These relays are controlled by the S and SA alarms. Alarm conditions are removed automatically when proper operation is restored.

5.3.7.2 Detailed Design

BITE, in conjunction with the BITE card, consists of sensors placed on each printed circuit card. These sensors are tri-state buffers and are connected to particular points on the printed circuit card that are known to be electrically active or in a certain logic state during proper operation. Each card contains 12 of these sensors, with the exception of the loop modems which contain 16, and the outputs of these buffers are bussed in the back plane wiring, i.e., the outputs of sensor 1 on each card are connected together, the outputs of sensor 2 are

TABLE 5-3. TIMING GENERATOR OUTPUTS

RLGM Configuration	-	4 1/2 Chan	-	-	-	-
LGM Configuration	8 Chan	9 Chan	-	-	16 Chan	18 Chan
RMC Configuration Input	4 1/2 Chan	4 1/2 Chan	-	-	8 Chan	9 Chan
RMC Configuration Output	8 Chan	9 Chan	8 Chan	9 Chan	16 Chan	18 Chan
Switch 1	1	1	0	0	1	1
Switch 2	0	1	0	1	0	1
Switch 3	1	0	1	0	0	1
<u>CLOCKS</u>						
* Station Clock, Recovered Clock, or Data Clock Input	256	288	256	288	512	576
* Output Group	256	288	256	288	512	576
* 2X Output Group	512	576	512	576	1024	1152
* 8X Output Group	2048	2304	2048	2304	4096	4608
* Input Group	144	144	144	144	256	288
* 2X Input Group	288	288	288	288	512	576
* 8X Input Group	1152	1152	1152	1152	2048	2304
* Loop Modem Clock 1	512	512	512	512	512	512
* Loop Modem Clock 2	64	64	64	64	64	64
* Loop Modem Clock 3	32	32	32	32	32	32
Group Framing Clock	32	32	32	32	32	32
Telemetry Clock	2	2	2	2	2	2
Timeout Clock	0.15	0.15	0.15	0.15	0.15	0.15

NOTES: 1. * Rates halve when 16 kb/s DSVT's are used

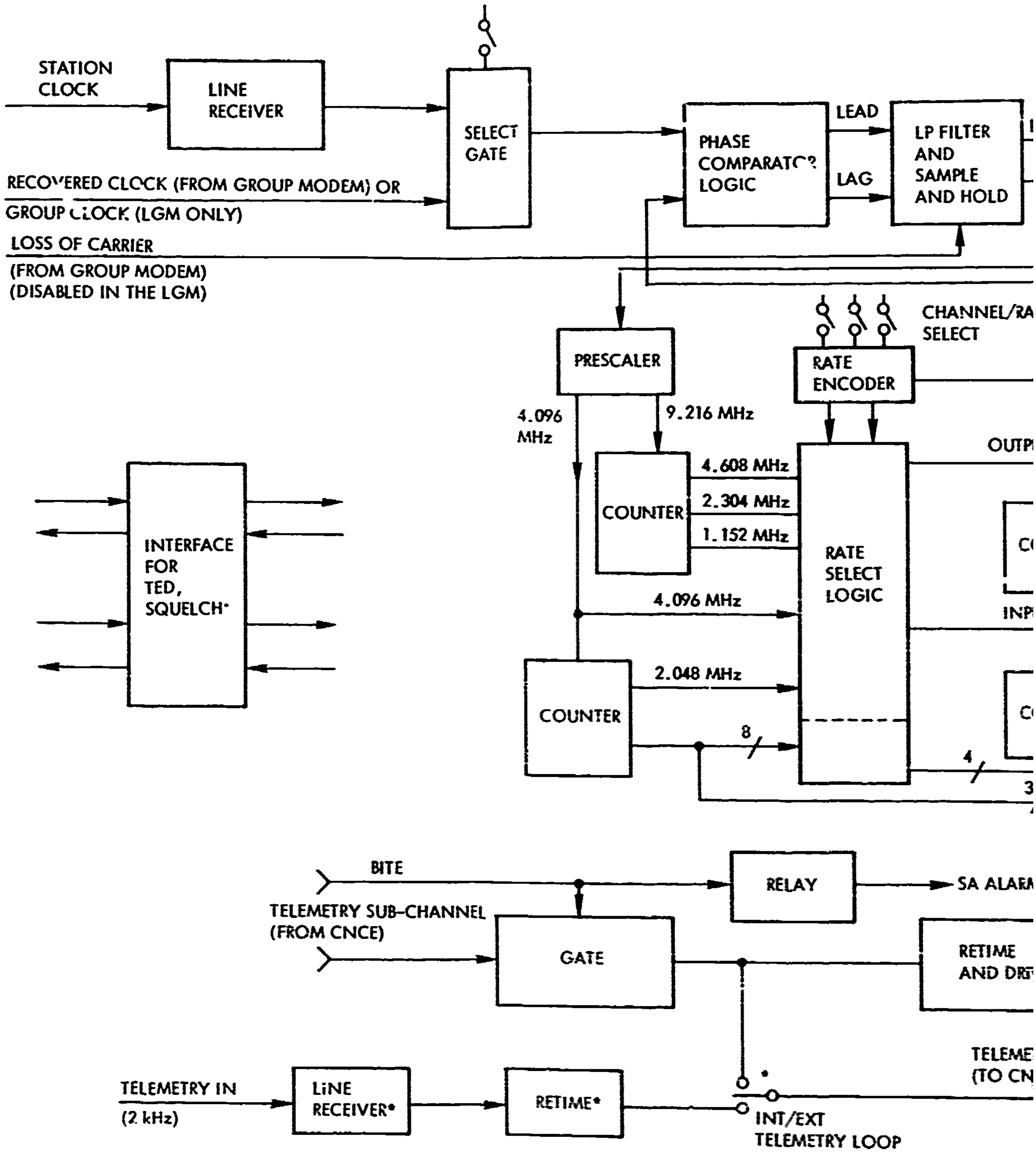
2. All rates are in KHz

connected together, etc. In this manner the buffers on one card can be enabled and the 12 or 16 points, of that card, examined for activity or a level and compared to what is defined for those points on that card. If any of the 12 or 16 bits of information are in error the card is examined again, one second later, if the error persists the card is declared in fault and the BITE light on that card illuminated.

The function of the BITE card is to control all the sequence timing and programming (by back plane wiring) information necessary to evaluate the sensor outputs for each card. It is also necessary for the BITE card to store which cards are in fault to maintain the individual fault lights until those cards can be checked again. A block diagram of the BITE card is shown in Figure 5-13.

During operation, the tri-state buffers are enabled on one card at a time and the 16 bus lines from the buffers applied to two eight bit multiplexers. Bits 0-7 are termed Group 1 and bits 8-15 Group 2. A counter controls the addressing of these multiplexers such that 2 bits are examined at a time, one from each group. This counter also addresses two additional multiplexers that contain the program information as to whether the monitored bits from Group 1 are to be electrically active or a specific logic level and as to whether they are an internal or external function. External is defined as any failure that can be attributed to a fault outside the unit, such as loss of clock or loss of diphase in. All bits from Group 2 are pre-defined to monitor electrical activity and defined to be internal faults so that no programming is necessary. Tables 5-4 to 5-9 define the specific functions which are examined by the BITE card for each card during the scan of Groups 1 and 2.

The outputs of the eight bit multiplexers are applied to error generating circuits that produce outputs when errors exist in the bit positions being examined. These errors are then 'OR'ed and Exclusive-'OR'ed and applied to a two-channel multiplexer. For all the cards, with the exception of a Loop Modem, the "OR" function is selected producing an error when one or both bits are in fault.



STATION CLOCK
LINE RECEIVER
SELECT GATE
RECOVERED CLOCK (FROM GROUP MODEM) OR
GROUP CLOCK (LGM ONLY)
LOSS OF CARRIER
(FROM GROUP MODEM)
(DISABLED IN THE LGM)
PHASE COMPARATOR LOGIC
LEAD
LAG
LP FILTER AND SAMPLE AND HOLD
CHANNEL/RA
SELECT
PRESCALER
RATE ENCODER
4.096 MHz
9.216 MHz
COUNTER
4.608 MHz
2.304 MHz
1.152 MHz
RATE SELECT LOGIC
OUTP
INTERFACE FOR TED, SQUELCH*
4.096 MHz
INP
COUNTER
2.048 MHz
8
4
3
BITE
RELAY
SA ALAR
TELEMETRY SUB-CHANNEL
(FROM CNCE)
GATE
RETIME AND DR
TELEME
(TO CN
TELEMETRY IN
(2 kHz)
LINE RECEIVER*
RETIME*
INT/EXT
TELEMETRY LOOP

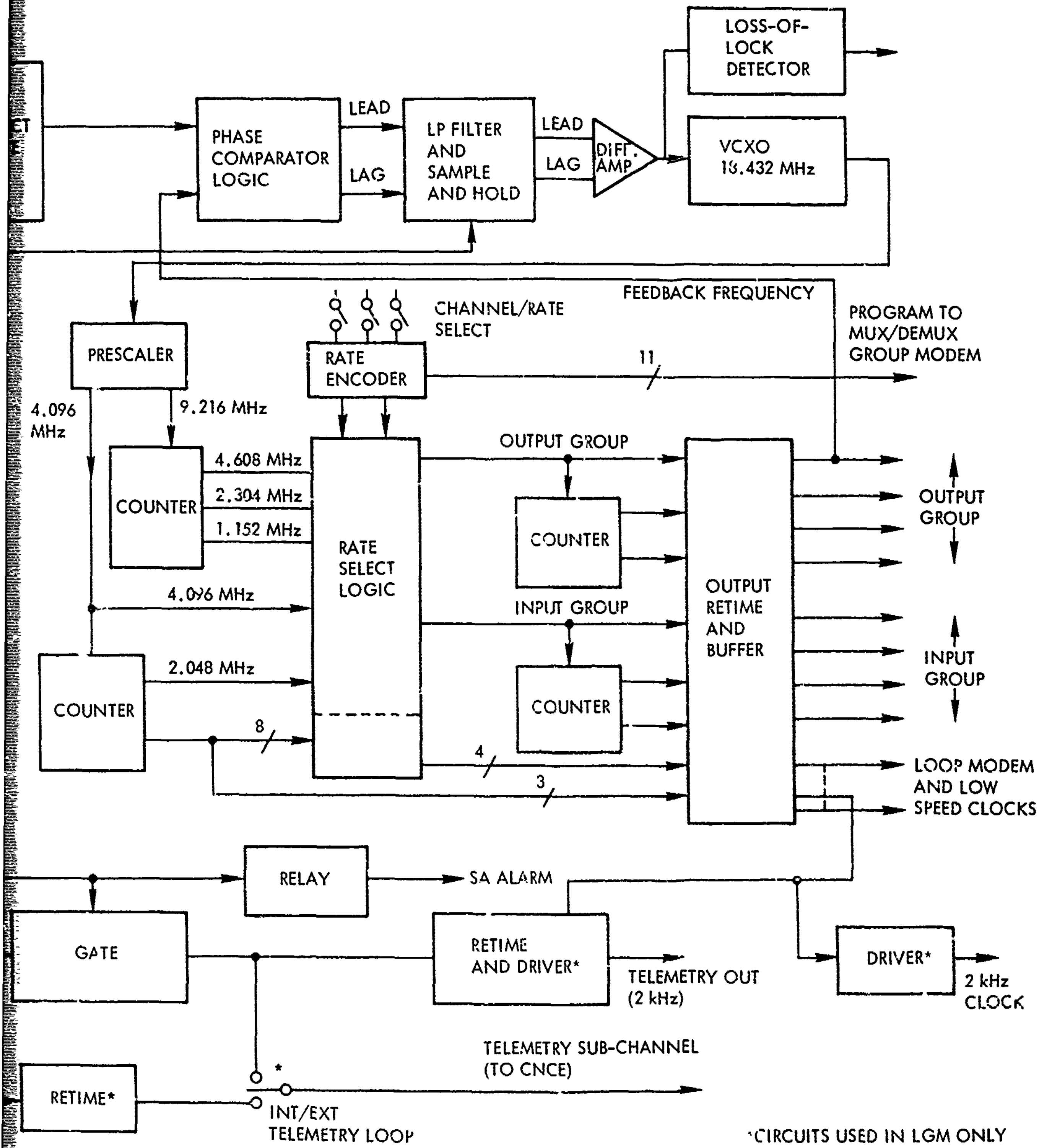
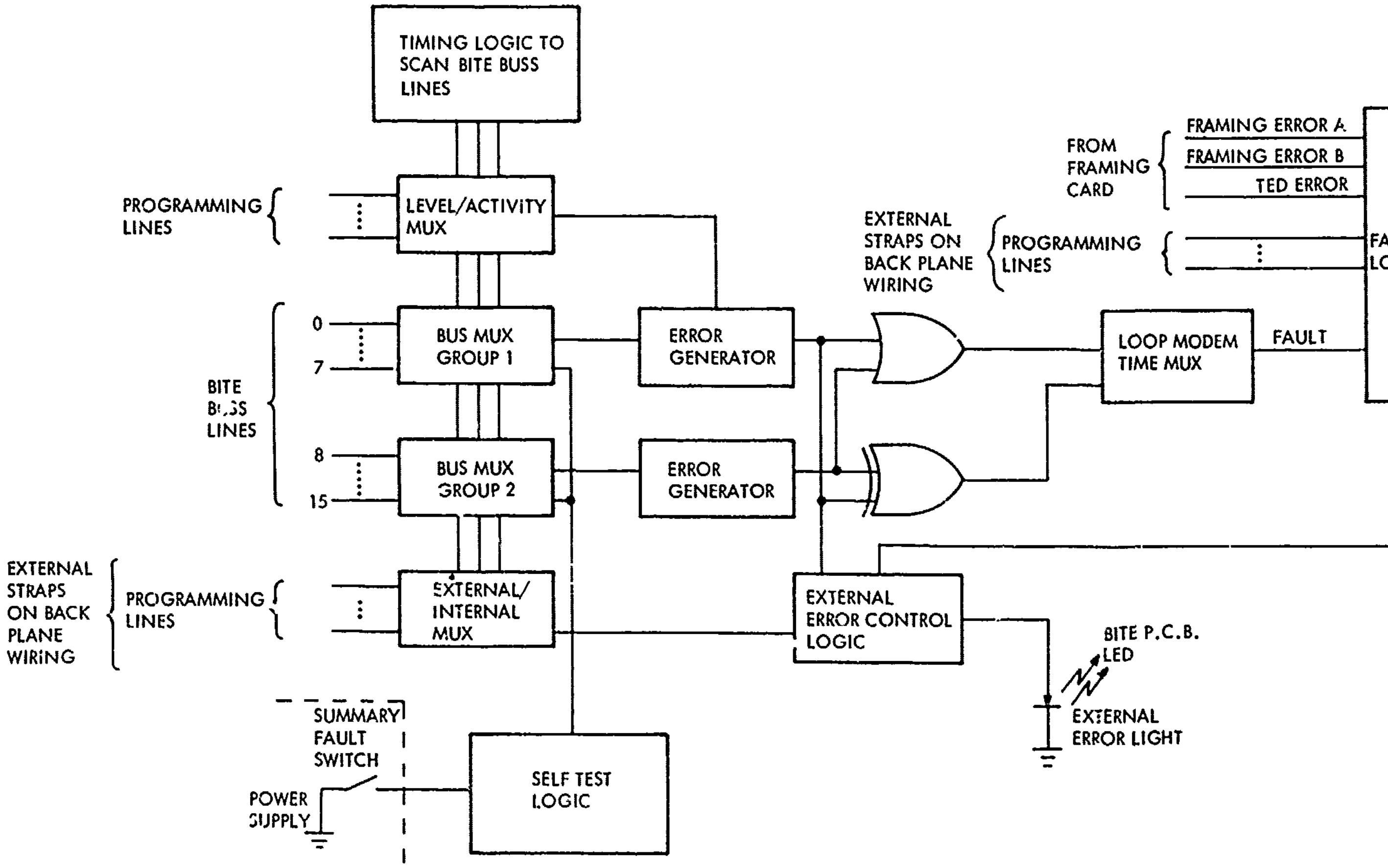


Figure 5-12. Timing Generator Block Diagram

2



TIMING LOGIC TO SCAN BITE BUSS LINES
PROGRAMMING LINES
LEVEL/ACTIVITY MUX
BITE BUSS LINES
0
7
8
15
BUS MUX GROUP 1
BUS MUX GROUP 2
ERROR GENERATOR
ERROR GENERATOR
EXTERNAL STRAPS ON BACK PLANE WIRING
PROGRAMMING LINES
EXTERNAL/ INTERNAL MUX
SUMMARY FAULT SWITCH
POWER SUPPLY
SELF TEST LOGIC
EXTERNAL ERROR CONTROL LOGIC
BITE P.C.B. LED
EXTERNAL ERROR LIGHT
EXTERNAL STRAPS ON BACK PLANE WIRING
PROGRAMMING LINES
FROM FRAMING CARD
FRAMING ERROR A
FRAMING ERROR B
TED ERROR
LOOP MODEM TIME MUX
FAULT
FAU
LO

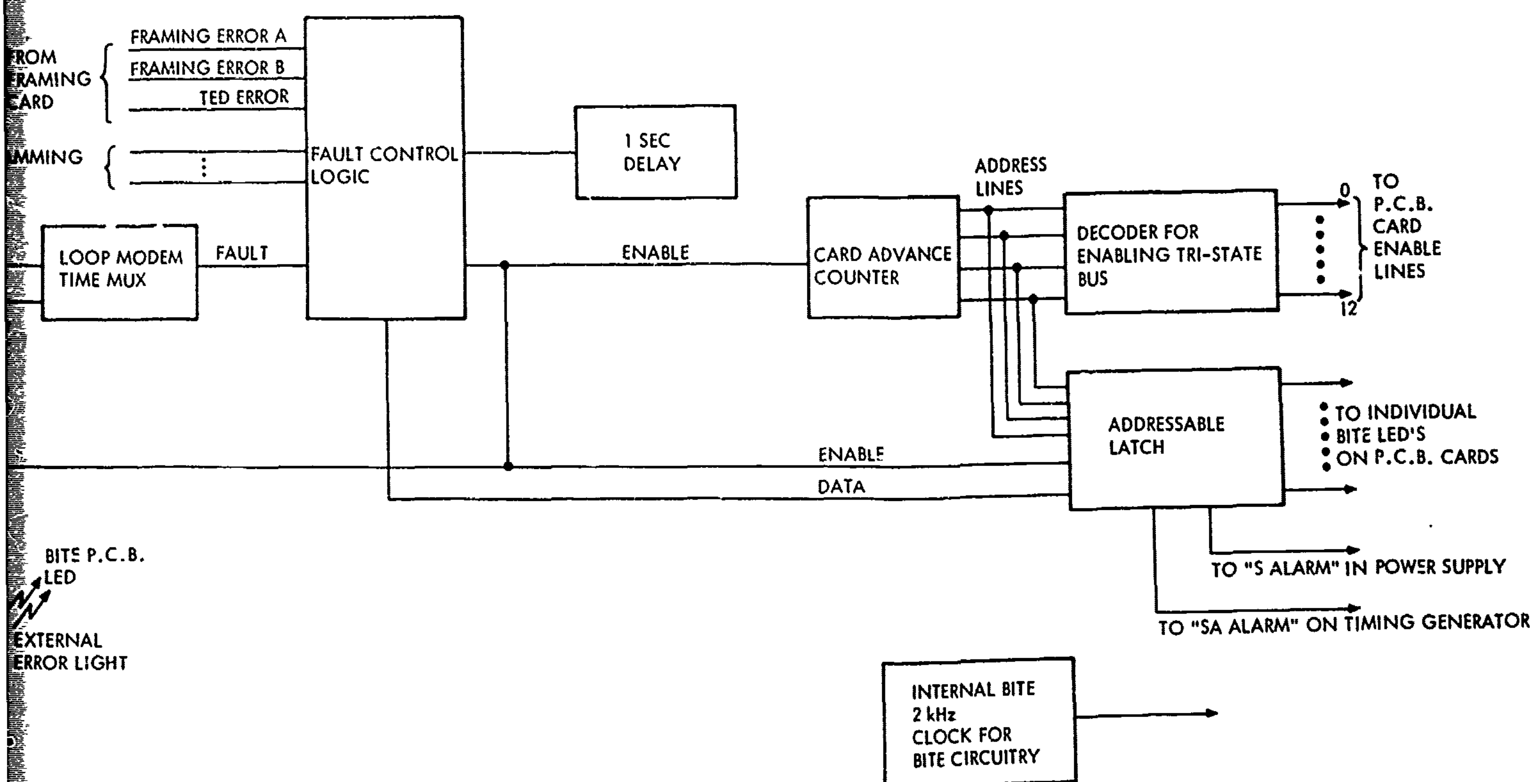


Figure 5-13. Block Diagram of BITE Card

2

TABLE 5-4. TIMING GENERATOR BUS ASSIGNMENT

BITE BUS	Int/Ext	Level/Activity	Signal Description
0	Ext	Act	Loss of station clock
1	Int	Level	Loss of clock phase lock
2	Int	Act	Phase Comparator
3	Int	Act	2K Hz clock
4	N. U.		
5	N. U.		
6	N. U.		
7	N. U.		
8	Int	Act	150 Hz clock
9	Int	Act	64K/32K Hz clock
10	Int	Act	512K/256K Hz clock
11	Int	Act	Input group clock
12	Int	Act	2 times input group clock
13	Int	Act	Output group clock
14	Int	Act	2 times output group clock
15	Int	Act	8 times output group clock

Ext = External Fault

Act = Sensor Detects Activity

Level = Sensor Detects Level

N. U. = Byte Not Used

TABLE 5-5. GROUP MODEM BUS ASSIGNMENT

BITE BUS	Int/Ext	Level/Activity	Signal Description
0	Ext	Level	Loss of Diphase Data in
1	Int	Level	Pullup level
2	Int	Activity	Recovered clock
3	Int	Level	Data phase correction
4	N.U.		
5	N.U.		
6	N.U.		
7	N.U.		
8	Int	Act	Recovered clock output
9	Int	Act	Base Band Data Out
10	Int	Act	Diphase Group Data Out
11	Int	Act	Phase Transition Data
12	Int	Act	Data sample clock
13	Int	Act	Data into Fifo
14	Int	Act	Digital phase lock loop feedback
15	Int	Act	Hardlimited diphase data

Ext = External Fault

Act = Sensor Detects Activity

Level = Sensor Detects Level

N.U. = Byte Not Used

TABLE 5-6. LOOP MODEM BUS ASSIGNMENT

BITE BUS	Int/Ext	Level/Activity	Signal Description	Loop Modem
0	Ext	Level	⊕ 8 Carrier Activity In	A
1	Ext	Level	⊕ 9 Carrier Activity In	B
2	Int	Act	Internal Clock	A
3	Int	Level	Power Feed Status	A, B
4	Int	Level	⊕ 12 Base Band Activity In	A
5	Int	Level	⊕ 13 Carrier Activity In	A
6	Int	Level	⊕ 14 Base Band Activity In	B
7	Int	Level	⊕ 15 Carrier Activity In	B
8	Ext	Act	⊕ D Diphase Out	A
9	Ext	Act	⊕ 1 Diphase Out	B
10	Int	Act	Internal Clock	A
11	Int	Act	Internal Clock	B
12	Int	Act	⊕ 4 Diphase Out	A
13	Int	Act	⊕ 5 Baseband Data Out	A
14	Int	Act	⊕ 6 Diphase Out	B
15	Int	Act	⊕ 7 Baseband Data Out	B

Note: There are 2 Loop Modems per card A and B

+ N - indicates exclusive 'OR'ed with byte N

TABLE 5-7. MUX/DEMUX BUS ASSIGNMENT

BITE BUS	Int/Ext	Level/Activity	Signal Description
0	Ext	Level	Failure to detect Data One
1	Int	Act	Demux enable pulse
2	Int	Act	Generation of overhead bit of mux
3	Int	Act	Activity of Demux address
4	N. U.		
5	N. U.		
6	N. U.		
7	N. U.		
8	Int	Act	Generation of Frame Bit
9	Int	Act	Cycling of overhead Mux counter
10	Int	Act	Group Data out of Mux
11	Int	Act	Cycling of Loop Mux counter
12	Int	Act	Cycling of Loop Demux counter
13	Int	Act	Overhead channel generator Demux
14	Int	Act	Frame reference generator
15	Int	Act	Data equal zero monitor

Ext = External Fault

Act = Sensor Detects Activity

Level = Sensor Detects Level

N. U. = Byte Not Used

TABLE 5-8. GROUP FRAMING BUS ASSIGNMENT

BITE BUS	Int/Ext	Level/Activity	Signal Description
0	Ext	Level	Frame squelch
1	Int	Level	Synchronizer in illegal state A
2	Int	Level	Synchronizer in illegal state B
3	Int	Level	Synchronizer in illegal state C
4	N. U.		
5	N. U.		
6	N. U.		
7	N. U.		
8	Int	Act	Pattern Type Counter
9	Int	Act	Pattern Type Recycling
10	Int	Act	Frame interval counters
11	Int	Act	Generation of frame intervals
12	Int	Act	Counting of frame counters
13	Int	Act	Counting of error counters
14	Int	Act	Loading of error counters
15	Int	Act	Counting of frame counters

Ext = External Fault

Act = Sensor Detects Activity

Level = Sensor Detects Level

N. U. = Byte Not Used

TABLE 5-9. INTERFACE CARD BUS ASSIGNMENT

BITE BUS	Int/Ext	Level/Activity	Signal Description
0	Ext	Level	Receive group data
1	Ext	Level	Receive group clock
2	Int	Level	Transmit group data
3	Int	Level	Transmit group clock
4	N.U.		
5	N.U.		
6	N.U.		
7	N.U.		
8	Int	Act	Fifo input enable pulse A
9	Int	Act	Fifo input enable pulse B
10	Int	Act	Fifo output enable pulse B
11	Int	Act	Master input enable pulse
12	Int	Act	Fifo input address
13	Int	Act	Group address Fifo output
14	Int	Act	Group address Fifo input
15	Int	Act	Fifo output group address

Ext = External Fault

Act = Sensor Detects Activity

Level = Sensor Detects Level

N. U. = Byte Not Used

For the Loop Modem, the Exclusive-OR function is selected producing an error only if one of the two bits being examined are in fault. This is an important feature of the BITE card because when a loop modem is not being used errors are produced in both bit positions, the Exclusive-OR prevents a failure indication. For example; if the two bits being examined, at one time, are diphase-activity-out and baseband-activity-in the only faults that will be recognized are diphase out with no baseband in, or no diphase out with baseband in. When the Loop Modem is not being used, there is no diphase out and no baseband in causing two errors, the Exclusive-OR indicating no fault.

The fault, if any, is then stored in gating logic until the completion of the 16 bits. In this logic the fault is inhibited if there is a previous fault on the Timing Generator card or output Group Modem. This prevents the indication of faults on all cards if there is a timing failure or a loss of diphase data in. The fault will be inhibited if the input group of the RMC is not being used and the card being examined is an input group Mux/Demux, Group Framing, or input Group Modem. The fault will also be inhibited if the error occurs in station clock activity and the clock and timing card is operating from recovered clock.

If the fault is not inhibited a one second delay is initiated and at the end of the delay the fault checked again. If a fault is still present the LED on that card is illuminated. The "card advance counter" is then advanced to examine the next card. If there is no fault on the card, the counter is advanced at the completion of examining the 16 bits, no delay is initiated, and any previous fault indication on that card will be removed.

The LED on the BITE card is designated as the "external fault" indicator and is illuminated if a bit (refer to Tables 5-4 to 5-9) designated as external is in fault for longer than one second.

5.3.7.3 Alarms

The BITE card generates two types of alarms referred to as the "S" and the "SA" alarms. The "S" alarm is the all inclusive or summary alarm. This alarm is active when any fault (internal or external) is detected. This alarm causes the summary error indicator located on the power supply front panel to illuminate and in addition causes a fault relay located in the power supply to de-energize causing a contact closure. The "SA" alarm goes to the alarm state for all internal or external errors except for Loop Modem and/or Frame Status errors. In the RMC, frame status includes both the input and output groups. The Resync Achieve (TED) status is not included in the SA alarm in the LGM in addition to the Loop Modem and/or Frame Status errors. This alarm causes a relay located on the Timing Generator to de-energize causing a contact closure. The "SA" alarm will also cause all zeroes to be generated in the Telemetry subchannel when active (alarm state). Figure 5-14 is a block diagram of the alarm implementation in the LGM. Figure 5-15 is a block diagram of the alarm implementation for the RMC and the RLGM.

The LED located on the BITE card illuminates only when an external error occurs.

Also built into the BITE card is self-test circuitry that is initiated by a switch closure on the front panel of the power supply (part of the Press-to-Test lamp). All existing faults are removed, errors are then introduced on all cards except the Timing Generator and output Group Modem. This causes all fault indicators to illuminate except those on the Timing Generator and output Group Modem. Errors are then introduced on all cards illuminating those LED's on the Timing Generator and output Group Modem and because of the fault inhibit logic extinguishing those on the other cards. The BITE card then returns to its normal operating mode.

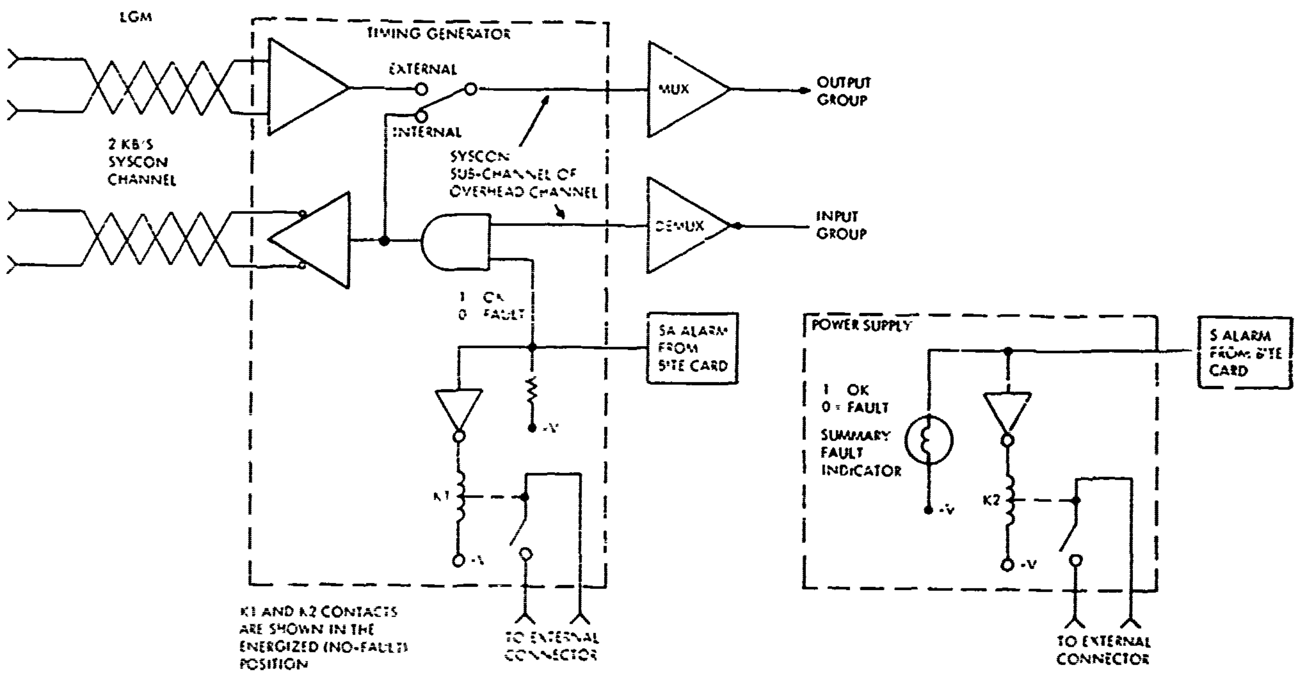


Figure 5-14. LGM Alarm Implementation Block Diagram

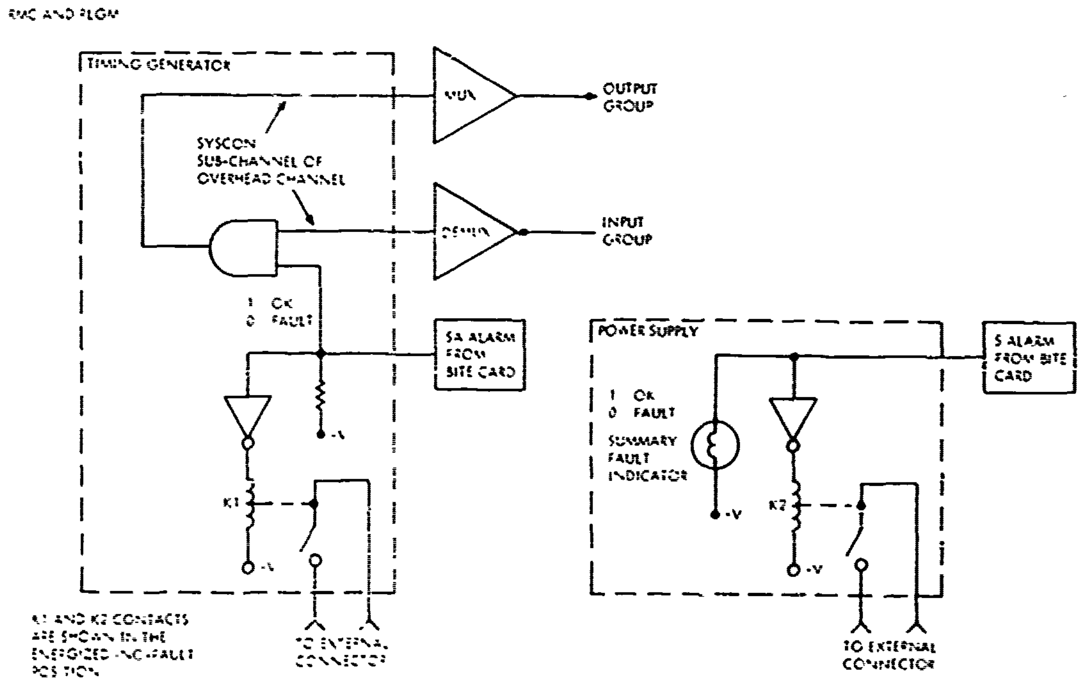


Figure 5-15. RMC Alarm Implementation Block Diagram

Tables 5-4 through Table 5-9 show the function of each bit of each card type, indicating whether the signal monitored is a level or activity and internal or external.

Table 5-10 illustrates the order in which the cards are examined in the RMC, RLGM and LGM.

TABLE 5-10. ORDER IN WHICH THE P.C. CARDS ARE SCANNED

Card #	Enabling Line	RMC	RLGM	LGM
1	BTEN0N	Clock & Timing	Clock & Timing	Clock & Timing
2	BTEN1N	Group Modem (High)	Group Modem	Interface Card
3	BTEN2N	MUX/DEMUX (High)	MUX/DEMUX	MUX/DEMUX
4	BTEN3N	FRAME/SYNC (High)	FRAME/SYNC	FRAME/SYNC
5	BTEN4N	Group Modem (Low)	Loop Modem (1)	Loop Modem (1)
6	BTEN5N	MUX/DEMUX (Low)	Loop Modem (2)	Loop Modem (2)
7	BTEN6N	FRAME/SYNC (Low)	NC	Loop Modem (3)
8	BTEN7N	Loop Modem (1)	NC	Loop Modem (4)
9	BTEN8N	Loop Modem (2)	NC	Loop Modem (5)
10	BTEN9N	Loop Modem (3)	NC	Loop Modem (6)
11	BTEN10N	Loop Modem (4)	NC	Loop Modem (7)
12	BTEN11N	NC	NC	Loop Modem (8)
13	BTEN12N	NC	NC	NC
14	BTEN13N	NC	NC	NC
15	BTEN14N	NC	NC	NC
16	BTEN15N	NC	NC	NC

5.3.8 Power Supply

5.3.8.1 Introduction

The Power Supply design represented a most significant technical challenge. The power supplies must have efficiencies of as high as 65% while at the same time be constrained within tightly controlled space and weight restrictions. For this reason, an extensive make/buy evaluation was undertaken. In this regard, there was generated a detailed power supply specification SM-A-876875 and Statement of Work. This power supply specification was submitted to ECCM.

5.3.8.2 RLGM Power Supply Design

5.3.8.2.1 Major Performance Requirements

The voltage and current requirements between the RLGM, RMC and LGM are very closely related. There is, therefore, a common requirement for both the shelter and field units. This similarity has resulted in a high degree of Power Supply commonality which has resulted in the utilization of common P.C.B.'s in each of the three units. A total of six P.C.B.'s will be required for these units. Table 3-11 shows the utilization, type, and electrical requirements of these modules.

Other performance requirements of the Power Supply are summarized in Table 3-12. These requirements are detailed in the Power Supply specification SM-A-876875.

5.3.8.2.2 Functional Description

A flyback type of converter is used for the DGM power supplies. This type of converter has been used quite extensively in space applications where high reliability and efficiency is a must. A brief description of the basic flyback operation and schematic is given in paragraph 3.3.8.3.2.

The RLGM power supply is comprised of modular blocks utilized extensively in the DGM family. A block diagram of the RLGM power is shown in Figure 5-16.

Prime power after being pre-conditioned by EMI filters and EMP arrestors is routed to the appropriate AC or DC input network via a relay controlled by a DC sensing circuit. The circuit is configured for AC operation in the non-energized mode; a long time constant prevents dropout, pre-charges the input DC/DC converter filter network to avert current surges through the relay, and prevents inadvertant DC polarity reversal. Figure 3-28 is a schematic of this circuit. A two pole circuit breaker is used on the input. The circuit breaker will break both sides of the line, but senses only the hot side of the line. Trip points will be set at 3 amps RMS for the 115 V AC operation, and at 15 amps DC for the 28V operation. Figure 3-29 shows the circuit breaker configuration.

Either the 28 VDC prime input is converted or AC is rectified into a nominal 160 VDC. This voltage is applied as source power to the flyback converters of the "B" and "H" modules which provide regulation and input/output isolation. When the RLGM is powered remotely, the input power is applied directly to the input of the flyback converters through a select switch. A separate ON/OFF switch is provided for the remote 180 VDC input. The power feed de-coupling circuits are located in the power supply and are mounted in the power supply chassis.

The "B" module converter transforms the high voltage (160 V) DC into pre-regulated DC outputs for subsequent utilization as load supplies, internal bias supplies, or regulation loop control. The "H" converter, converts the 160 V input to a regulated +55 VDC for transmission as source power to the DSVT's. Various operating conditions such as over and under voltage are monitored.

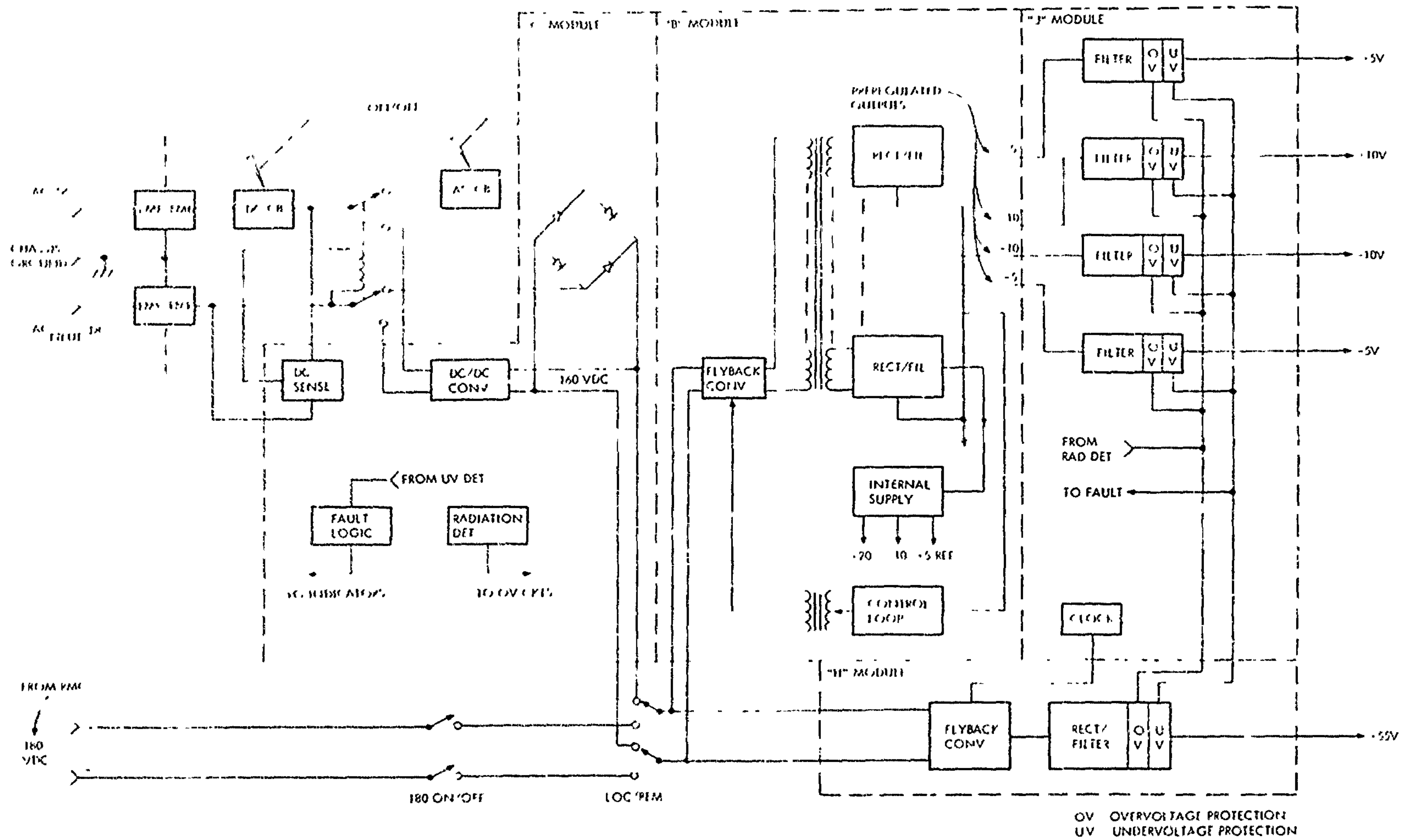


Figure 5-16. RGLM Power Supply Block Diagram

The RLGM internal load supplies are further conditioned by filters and monitored for out-of-tolerance performance and subsequent indication. Separate series regulators are not required since the DC internal load within the RLGM is low. Consequently, the logic load current variation is minimal. The transformer regulation loop is sufficiently "stiff" to maintain the ± 5 VDC and ± 10 VDC outputs within the specified regulation range.

Each output status is reported via the undervoltage (UV) summary combiner of the fault logic circuit. An overvoltage (OV) condition is crowbarred to protect the load and consequently appears as a UV anamoly following cessation of the OV indicated output. Impringing radiation is detected by a radiation circuit which initiates all crowbars, internal and external. to safeguard the load and the power supply.

5.3.8.2.3 PC Card Complement

The power supply modules which are used in the RLGM are as follows:

Module Type	Function
J	Consists of the ± 5 VDC and the +10 VDC limited range supplies, overvoltage circuits, undervoltage circuits, a clock, power down circuit and some components for the +55 and +180 VDC circuits.
B	Consists of the internal supply and pre-regulators for the series pass supplies.
C	Consists of the DC/DC converter, the radiation detector, and fault logic components.
H	Consists of the 55 V DC at 1.5 amp circuitry.

5.3.8.2.4 Technical PC Board Description

5.3.8.2.4.1 Module "C"

This card, shown schematically in Figure 3-30, contains the AC bridge rectifier, the DC/DC converter, the fault logic, and the radiation detector. The DC/DC converter is relatively straightforward, although it incorporates a feedback drive with clocked turn-off to facilitate efficiency in drive power and to minimize filter size by guaranteeing a fixed chopping frequency. An interlock assures simultaneous conduction does not occur.

The radiation detector is enabled when the 2N2222 conducts under nuclear bombardment, triggering the monostable. The fault logic combines the UV and test inputs to control the fault relay, fault lamp and power tolerance lamp.

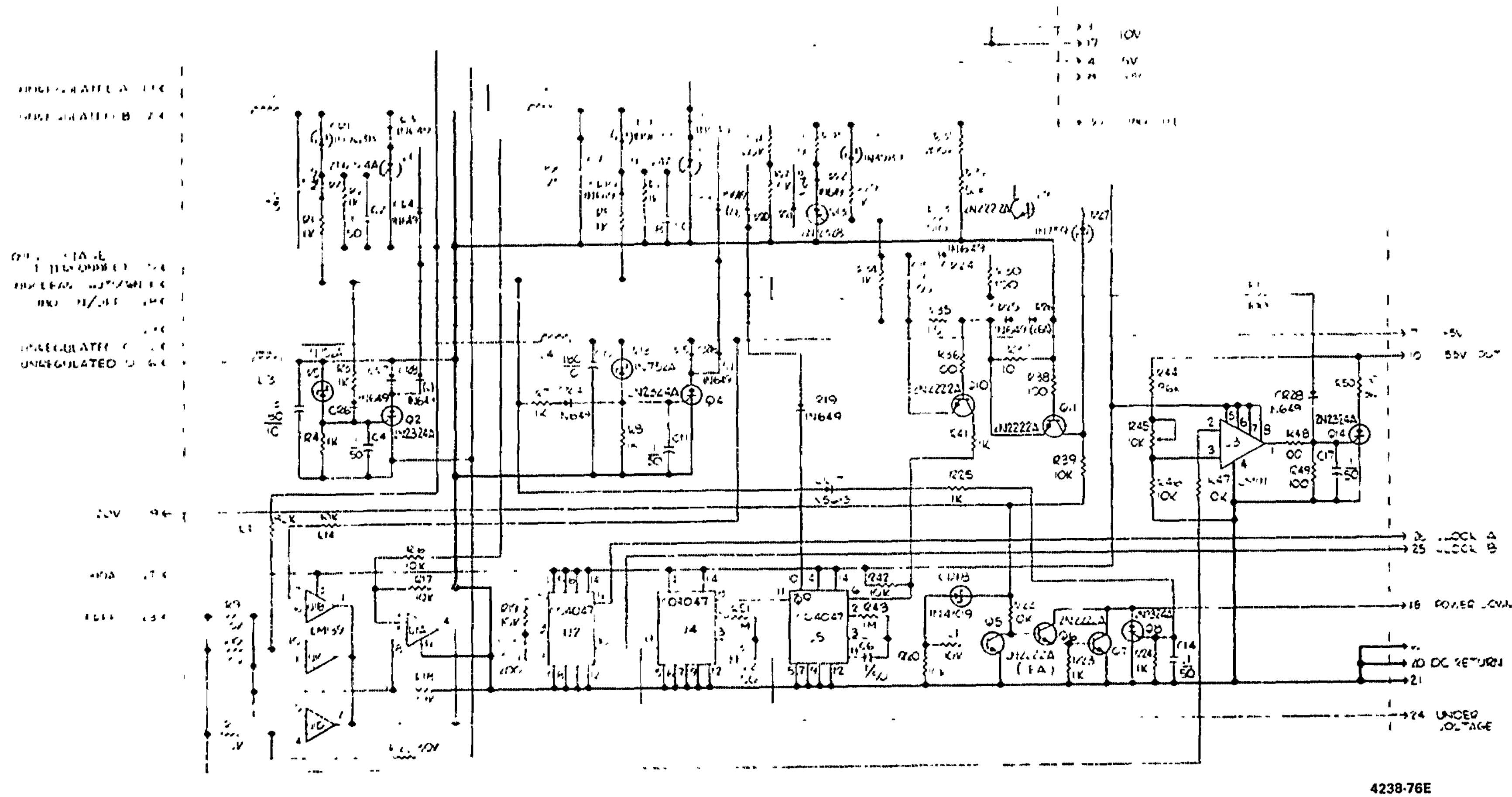
5.3.8.2.4.2 Module "B"

The schematic in Figure 3-31 depicts the flyback converter with its associated control loop and the resultant regulated outputs. This converter employs proportional base drive for efficiency and clocked cycle drive for frequency stability. Source overvoltage protection inhibits operation under input voltage duress and a startup circuit provides reliable initiation. The basic tenent is that energy stored in the primary inductance of the transformer during conduction of the power transistor is transferred to the secondaries when conduction ceases in response to either the regulation loop on a high current sensor. Thus, the circuit is energy limited and behaves, in principle, like the "electric ram".

The secondary outputs are rectified and filtered: some supply the loads, one is used for control feedback, and one generates the +20V, +10V, and +5V reference utilized for internal bias and control.

5.3.8.2.4.3 Module "J"

Refer to Figure 5-17 for the schematic for the "J" Module. The module contains additional filtering for the pre-regulated outputs from the "B" Module. The output of this module is the ±5 and ±10 VDC. Overvoltage and undervoltage



NOTES: UNLESS OTHERWISE SPECIFIED
1. ALL CAPACITOR VALUES ARE IN MICROFARADS AND VOLTS.
2. ALL RESISTOR VALUES ARE IN OHMS AND ARE ¼ WATT.
3. ALL CHOKES ARE SM-A-8765

Figure 5-17. Power Supply - Module "J"

protection is provided for each voltage output. In addition, a power down circuit is provided for powering down the supply in the event of adverse bias or during radiation conditions.

5.3.8.3.4.4 Module "H"

This card, see Figure 3-33, is a flyback converter for generating +55V to power the DSVT's and the operational description is synonomous with module "B", Section 3.3.8.3.4.2. The auxiliary overvoltage and start circuitry are unnecessary since the remainder of the supply accomplishes these functions indirectly on other cards. This module does make provisions for adjustable output and overvoltage sense point because of the close tolerances involved.

5.3.9 Signal Entry Panel

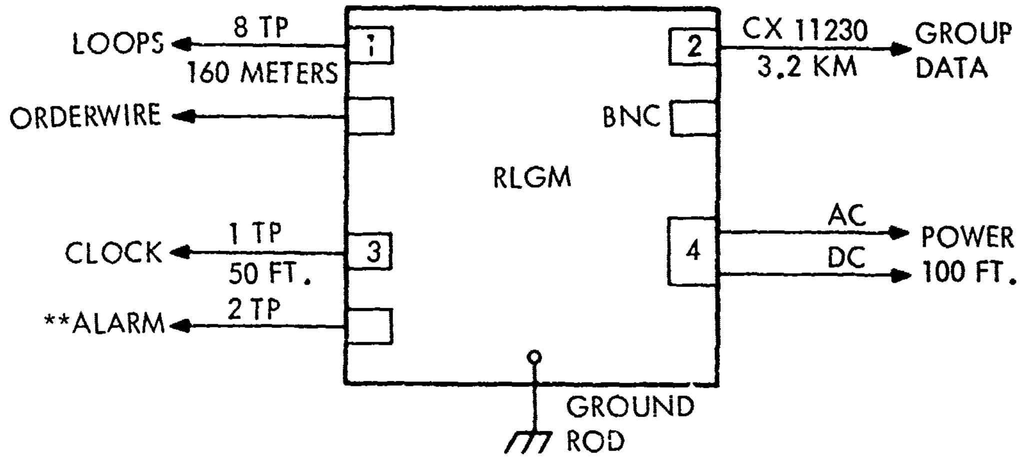
The cable interface for the RLGM and RMC is shown in Figure 5-17. A threat analysis has shown that both primary and secondary protection was necessary for these lines. It should be pointed out that pick-up on one cable drives current into all the external cables. This is because the ground rod impedance is not zero, and substantial voltages can be present between the case and ground.

The worst case threat is due to lightning. Previous studies on the effects of lightning have shown that the average lightning stroke reaches a peak current of 20,000 amps and a half period of 50 μs.

Based on this threat the following protective devices were chosen for the various types of interfaces in the RMC and RLGM units. These interfaces are: (numbers refer to interface line types of Figure 5-18).

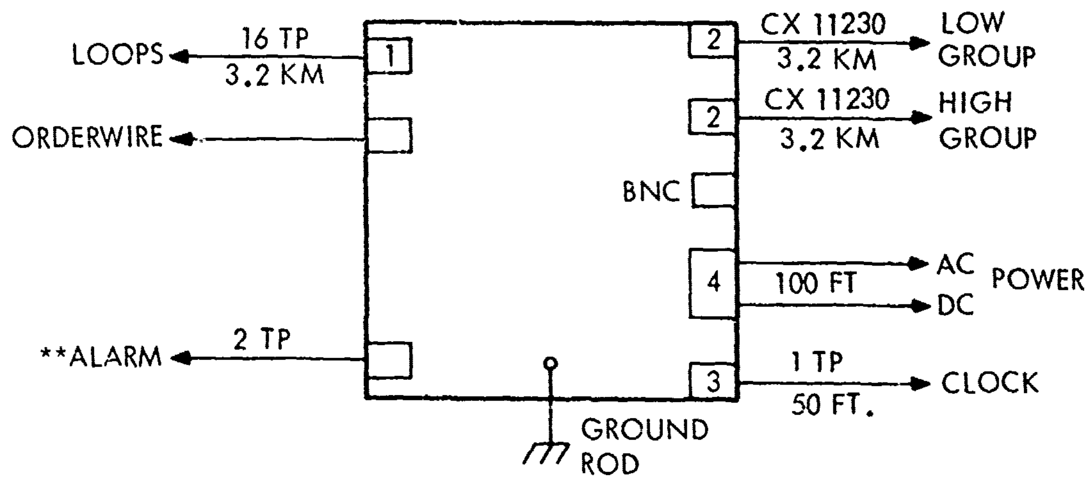
1. Diphase Loops
2. Group Data
3. Balanced Low Level Digital Interface
4. AC/DC Power

REMOTE LOOP GROUP MULTIPLEXER



**RELAY CONTACT

REMOTE MULTIPLEXER COMBINER



** RELAY CONTACT

8183-75E

Figure 5-18. Remote Loop Group Multiplexer and Remote Multiplexer Combiner

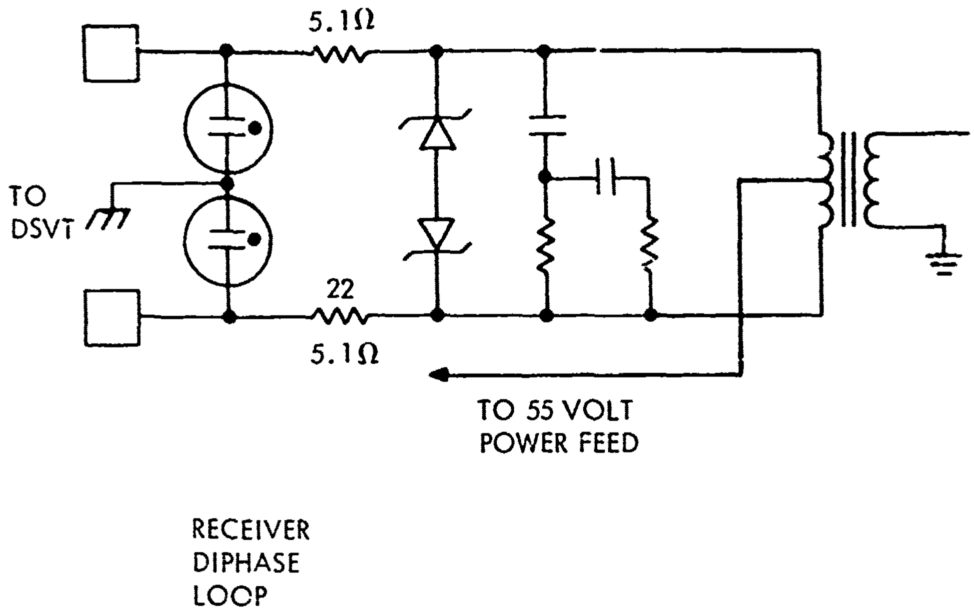
5.3.9.1 Diphase Loop Protection

The external cable for the loops is a 4 wire WF16 Field wire. The maximum length is specified at 3,200 meters. It is assumed that a direct lightning hit on this cable will divide evenly between all four wires placing a peak current threat to the unit of 5,000 amps per wire. As the primary protection we are using a Siemens gas filled surge arrestor model A3-C350. This unit has a rated surge discharge current of 10,000 amps. One protector is placed across each incoming wire to case ground. They are mounted as close to the signal entry panel as possible. All connections are kept as short as practical. Figure 5-19 shows the Diphase Loop receiver and transmitter interface respectively. Second level protection is provided by the diodes across the primary winding of the input transformer. Current limiting is provided by the 5.1 ohm resistors in series with each line.

5.3.9.2 Diphase Group Protection

The group data interface cable is a type CX11230. This is a dual coax cable with an outer shield. The outer shield will provide protection and reduce the threat to each of the coax lines. However, there is sufficient transfer impedance to warrant using surge protectors on each of these lines. A Siemens type A3-C350 is placed across each coax and coax shield to case group as shown in Figure 5-20.

These lines are designed to carry 180 VDC power to other remote units. Once a spark gap fires due to an EMP or lightning transient, the DC on these lines will tend to sustain the arc. In order to prevent this the 180 VDC power supplies are designed to reduce the output voltage to near zero in the overload condition. This extinguishes the spark gap and the system can return to normal operation. This power supply requirement applies to the RLGM Cable Driver designed by Raytheon.



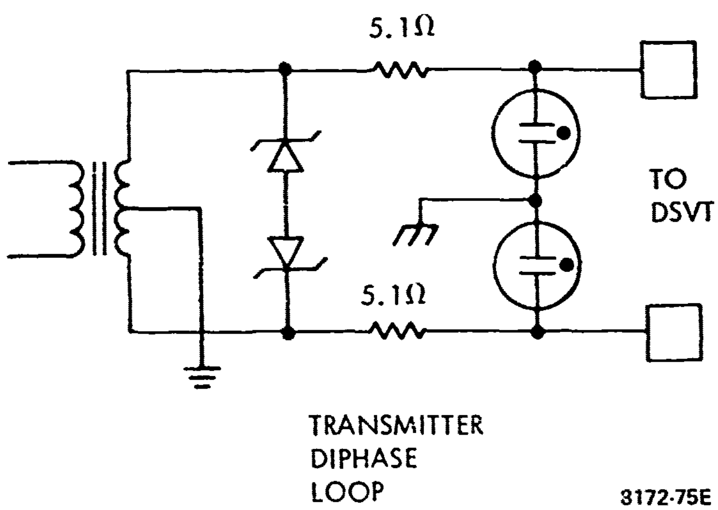


Figure 5-19. Receiver Diphase and Transmitter Diphase Loops

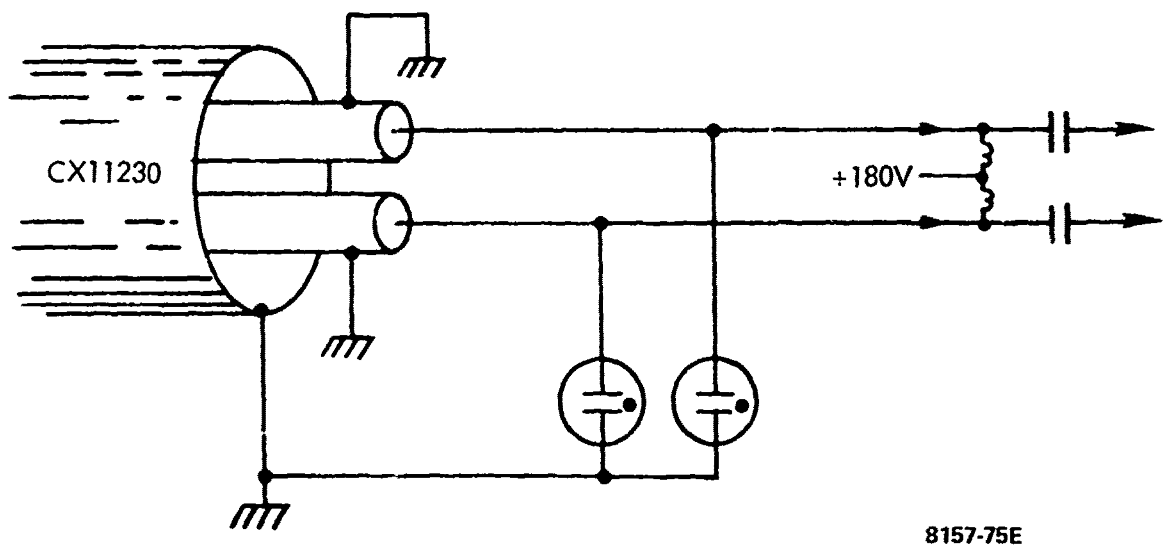


Figure 5-20. Group Data

5.3.9.3 Balanced Low Level Interface Protection

No protection is provided on Low Level Balanced Interfaces. It is assumed that the clock and alarm signals will be connected only when the RLGM or RMC is employed in a shelter or van in which case no protection is needed. Protection is not provided on the Orderwire Interface.

5.3.10 Human Factor Engineering

The RLGM design incorporates the requirements of MIL-STD-1472B to the maximum extent possible, consistent with operational requirements and physical design limitations imposed by TT-B1-2202-0013 performance specification.

Initial setup controls required to configure the equipment to system requirements are mounted on the accessible edge of the PCB's. These controls are protected by the front panel cover. The unit BITE control and alarm are positioned for rapid recognition and ease of identification.

Connections are located on the rear of the case and are positioned to ensure maximum accessibility.

Unit weights imposed by the specifications are within the requirements of MIL-STD-1472B for lifting and carrying.

Refer to section 15.4 of this volume for detail layouts of the RLGM mechanical assembly.

5.3.11 Reliability Design

The RLGM has a specified MTBF of 4000 hours. This is equivalent to 250 failures in 10^6 hours.

The reliability prediction and demonstrated results are summarized in Table 5-11.

TABLE 5-11.

RLGM RELIABILITY

Specified MTBF (Hrs)	Predicted MTBF (Hrs)	Demonstrated MTBF (Hrs)
4000	8915	13,600

5.3.12 Summary of PQT Results

The RLGM met or exceeded all major functional and environmental requirements. It is to be emphasized that the RLGM has successfully passed all of the above tests, as well as all interoperability tests and the out-of-spec conditions found during testing are all of a minor nature and do not affect interoperability. The out-of-spec characteristics are summarized below:

a. Loop output impedance: too high due to upper losses in coupling transformer.

b. Group signal fall time: one unit only, due to a faulty part.

c. Group Interface Input Impedance: out of spec at low frequency due to DC blocking capacitor used for protection of input.

d. RLGM input power: above the requirements established by the DGM Family ICD but not above prime specification.

e. Orderwire Input/Output Impedance: The copper losses in the coupling transformer were higher than expected.

5.3.12.1 Problems/Solutions

The problems encountered during the testing of the RLGM were not major and do not affect the mission of the equipment. Some of the problems, such as the Loop Modem output impedance, are common to the LGM and RMC. Most of the problems are at the interfaces where the RLGM interoperates with other equipment. Although the units interoperate properly, the interface specifications are not all met. Many specifications are too conservative and represent too pessimistic a view of the interface requirements for proper operation. The problems are presented below.

5.3.12.1.1 Loop Channel Output Impedance

The requirement in electrical characteristics testing for loop channel output impedance (Paragraph 11.12, Step 2 and 6 of F001) is that the output impedance be 125 ohms $\pm$ 15% at 8, 16, 32 and 56 KHz. This requirement is also in the DGM Family Interface Control Drawing 910669, Paragraph 1.4.1.b.

The impedances measured between 129.2 ohms and 164 ohms. The impedance out of tolerance is due to copper losses in the output coupling transformer and can be corrected by changing a series output resistor per loop channel (R38 and R50) from 120 to 91 ohms. This change would bring the impedance in specification.

There is no need to change the loop output impedance at this time as it does not impair the ability to use the DSVT. The multiplexer (RLGM) operates error free for all cases of cable length and frequency with the DSVT.

For this contract a waiver has been requested (waiver No. 029 - Loop Channel Output Impedance) due to the large quantity of printed circuit boards (413) that would have to be changed and the extensive retesting that would have to be done. The change would be incorporated in a subsequent contract.

5.3.12.1.2 Group Signal Fall Time

The requirement for group output signal fall time in electrical characteristic testing (F001), paragraph 11.20.3, Step 14 and paragraph 1.2.1.d of the DGM Family Interface Control Drawing is 130 ns measured 10% to 90% when terminated in 58 ohms. The fall time of one RLGM, serial number 15, measured 140 ns or 8% above specification. The failure was caused by a slow line driver on the Group Modem printed circuit board.

At the conclusion of electrical characteristics testing a waiver was generated (waiver no. 034 - Group Output Fall Time) to allow the use of this unit until the time the unit is returned to Sylvania for refurbishment. When the unit is refurbished the line driver SM-A-838261-1 will be replaced and the unit retested for rise and fall times. It is to be noted that of the 12 group interfaces tested in RLGM's and RMC's only this one failed the fall time requirement.

5.3.12.1.3 Group Interface Input Impedance

The requirement for group interface input impedance at the time electrical characteristics tests were performed was 58 ohms ± 15% from 300 Hz to 3 MHz. This requirement is Paragraph 11.21.3, Step 4 of F001 and Paragraph 1.2.1.3 of the DGM Family Interface Control Drawing. At 300 Hz the impedances are out of specification measuring as high as 78.5 ohms. This failure is due to a series blocking capacitor in the power supply which is used to isolate the 180 volt power feed on the cable from the Group Modem printed circuit board. At 300 Hz the reactance of this capacitor is large enough to force the impedance out of specification.

Because of the needed breakdown voltage (200 VDC) the capacitor must be physically very large and there is no room within the power supply to use a larger capacitor. The requirement for input impedance, therefore, has been respecified in the DGM Family Interface Control Drawing to 100 ohms maximum 300 Hz to 1 KHz; 58 ohms ± 15% 1 KHz to 3 MHz. The current design does not affect any other specification or impair the group signal or orderwire performance.

5.3.12.1.4 RLGM Input Power

The requirements for maximum power to the RLGM at the time electrical characteristics tests were performed was 40 watts for all sources of input (ac, dc and dc power feed). This requirement is Paragraph 11.10.3 of Electrical Characteristics Tests F001 and Paragraph 3.1.2.4.5 of the RLGM Prime Item Development Specification 11200C.

The original specification for maximum power was 60 watts as part of the Performance Specification Family of Digital Group Multiplexers TT-B1-2202-0013A dated 4 September 1975, Paragraph 3.2.1.3.6. Because of the power feed requirements placed on the RLGM input and the RMC output it was impossible for the RMC to supply 60 watts of power to the RLGM through 2 miles of cable due to the large dc resistance of the cable. At that time it was estimated that the RLGM would not require any more than 40 watts for power feed operation so the specifications were changed to 40 watts for power feed and also for ac and dc operation.

The requirement for 40 watts maximum is not adequate. The specifications 11200C Prime Item Development and 910669 DGM Family Interface Control Drawings are to be changed to the following:

RLGM Input Power

ac	115 volts $\pm 10\%$, 1 phase 50-400 Hz $\pm 5\%$	50 watts
dc	$+28 \begin{smallmatrix}+4 \\ -6\end{smallmatrix}$ volts	60 watts
Remote	$+180 \begin{smallmatrix}+16 \\ -40\end{smallmatrix}$ volts	43 watts

5.3.12.15 Orderwire Input/Output Impedance

Paragraph 11.22.3, Steps 4 and 9 of Electrical Characteristics Tests F001, Paragraph 1.7.B of the DGM Family Interface Control Drawing 910669 and Paragraph 3.1.2.4.2 of the RLGM Prime Item Development Specification 11200C require that the orderwire input/output impedances be 600 ohms $\pm$ 10%.

The input and output impedances ranged from 682 ohms to 710.8 ohms. The failure is caused by failure to make allowance for the copper

losses in the orderwire transformers at the time of the design. What is needed to bring the impedances within the limits of the specification is to change two series resistors, one for the output impedance and one for the input (R13 and R19), from 560 ohms to 470 ohms on the Group Modem CCA.

For this contract a waiver has been requested (waiver no. 032 - Orderwire Input/Output Impedance) to allow the use of the RLGM as is because the ability to use the COU is not affected. The current design meets the requirements of orderwire insertion loss Paragraph 1.7 Table IV of 910669 when interfaced with all the applicable equipment of the DGM Family. Changing the impedance on both ends of an orderwire link over two miles of cable would only improve the insertion loss by 1.5 dB out of 40 dB. To incorporate the change would require shipment, document changes, changing the resistors, rework of conformal coating and testing of the 57 printed circuit cards. The resistors could be changed on a production contract.

SECTION 7
RMC

The Remote Multiplexer Combiner (RMC) is used in tactical communications field locations (exposed) and also in shelters and vans. Its primary function is the time-division multiplexing of digital channels (loops) into a loop group and the combining of a group input from another unit with the loop group to form a higher capacity group. Built-in test equipment (BITE) facilities are provided to support operation and maintenance.

The Group Modem transmits and receives conditioned diphase group signals on the cable connecting the RMC to an interfacing DGM equipment. The group framing and synchronization element generates and detects the frame synchronization patterns required to maintain link synchronization. Frame synchronization is initiated when the out-of-sync condition is detected. The Multiplex-Demultiplex element time-division multiplexes 32 kb/s (or 16 kb/s) signals into a 4-1/2, 8 or 9-channel low group signal of 144, 256 or 288 kb/s. Inversely, it demultiplexes this group into its component channels for input to the high group RMC Multiplex-Demultiplex element that generates the 256, 288, 512, or 576 kb/s group signal. It also generates the groups overhead channel which contains framing and telemetry subchannels. An analog voice orderwire is provided on the low and high group channels for set up and maintenance of cable systems utilizing CX -11230 cable.

The DSVT loop input to the RMC interfaces with its Loop Modem elements. The Loop Modem element transmits and receives 32 kb/s (or 16 kb/s) conditioned diphase signals on the cable connecting a DSVT to the RMC. On its equipment side, 32 kb/s (or 16 kb/s) NRZ signals are exchanged with the associated Multiplex-Demultiplex element. This element multiplexes the 32 kb/s (or 16 kb/s) signals from the Loop Modem elements and combines them with the 32 kb/s (or 16 kb/s) signals obtained from the 144, 256, or 288 kb/s group input to the RMC into a

bit-interleaved group output of 256, 288, 512, or 576 kb s. Inversely, it demultiplexes this group, received from an interfacing DGM equipment, into its constituent channels so that the RMCs loop and group signals may be obtained. This Multi-Demultiplex element also generates the group overhead channel containing sub-channels for framing and telemetry information. The associated group framing and synchronization element generates and detects the frame synchronization patterns required to maintain synchronization on the group output link. Frame synchronization is initiated when the out-of sync condition is detected on this link. The Group Modem element exchanges balanced NRZ group output signals with the Multiplex-Demultiplex element and transmits and receives the conditioned diphase group output signal on the cable connecting the RMC to an interfacing DGM equipment.

The Timing Generator element generates the internal timing/clock signals required by the RMC elements. BITE monitors RMC performance and provide fault detection and isolation. RMC DC power is obtained from its Power Supply element which operates from ac or dc primary power sources. This element also feeds power to the RMCs interfacing loop (DSVT) and low group (RLGM) input signal sources.

7.1 DESIGN GOALS AND REQUIREMENTS

The RMC function requirements are summarized in Table 7-1.

The major design objectives in the RMC was to reduce the number of P.C.B.'s required in the unit. Preliminary layouts of the unit showed that this unit would be very tightly packed. This was due primarily from the sizes of the transformers for both the EOW group and loop modems making these cards two slot (0.9 inch) P.C.B.'s. Because of these transformers, coupled with the space restrictions within the field units, the components were mounted on the right side of the P.C.B. therefore, all DGM P.C.B.'s are fabricated with the components mounted on the right side.

TABLE 7-1. FUNCTIONAL REQUIREMENTS - REMOTE MULTIPLEXER COMBINER (RMC)

Definition: The RMC shall time division multiplex full duplex digital channels into a single serial bit-interfaced group and demultiplex a group into individual channels. The RMC also combines a group input with a group formed by multiplexing local loops and decombine the received groups to provide a group output. The RMC shall feed power, via the cable, to an RLGM and via the field wire to the DSVT's.

	Loop Side	Low Group (to RLGM or RMC)	High Group Side
Type of Channels:	4 wire full duplex	Same	Same
Number of Channels:	4 or 7 or 8	4, 5/8/9	8/9/16/18
Bit Rate:	32/16 kb/s	72/128/144/256 288 kb/s	128/144/256/ 288/512/576 kb/s
Modulation:	Conditioned Diphase	Conditioned Diphase	Conditioned Diphase
Used With:	DSVT	RLGM or RMC	RMC, Group Modem
Cable Type:	WF-16 field wire	CX-11230	CX-11230
Distance:	--	3.2 km	3.2 km
Power Feed:	DSVT per TT-A3-9002-0017	RLGM (60 watts max)	None
Impedance:	125 ±10%. Return loss ≥ 26 dB in the band from 8 to 56 kHz		
Orderwire:	--	Analog Voice (Maintenance)	Analog Voice (Maintenance)
Termination:	4 binding posts for each loop	UG-1837/U	UG-1837/U
Timing:	External station clock or derived from the received high group signal. Loss of received group signal for 0.5 seconds shall not cause loss of BCI.		

TABLE 7-1. FUNCTIONAL REQUIREMENTS - REMOTE MULTIPLEXER COMBINER (RMC) (Cont.)

Overhead Channel Structure:	Group Output (high group); eight subchannels, first channel is framing, second is RMC telemetry, third and fourth are other telemetry. Transpose third to second and fourth to third on Group input; first is framing subchannel			
Modularity:	Loops	RGLM	RMC	Output (Combined Group Side)
	3	144 kb/s	--	256 kb/s*
	4	144 kb/s*	--	288 kb/s*
	7	--	288 kb/s	512 kb/s*
	8	--	288 kb/s*	576 kb/s*
	8	--	--	288 kb/s*
	*Halve rates for 16 kb/s operation			
Size:	8.5" H x 13" D x 17.5" (without transit covers) may be rack mountable by adding bracketry supplied by government			
Input Power:	400 watts maximum			
Type of Power:	115 VAC $\pm$10%, 50 to 400 Hz or +28 VDC $^{+4}_{-6}$ volts			
Weight:	21.2 KG (46.6 lbs) maximum (without transit covers)			
BITE:	Power Monitor/Fault Isolation			
Reliability:	2500 HR-MTBF			

7.2 DESIGN APPROACH

7.2.1 Summary

There are a number of basic design approaches which the subcontractor used throughout the design of the RMC to optimize commonality with the Raytheon units. Basic design approaches were as follows:

a. The extensive use of C-MOS devices (refer to 3.2.1)

b. The use of common printed circuit boards between the field and shelter units

c. Minimized the design of the loop modem circuit so that two loop modem's could be packaged on a single P.C.B.

d. Designed the power supply so that common circuit designs are used in the field and shelter units

e. Designed the Power Supply form factor so that it is identical with the RLGM

f. Designed the loop modem P.C.B.'s so that they were completely interchangeable with the loop modem P.C.B.'s used in the shelter units

g. Designed the Group Modem P.C.B. so that it is completely interchangeable with the Group Modem P.C.B. used in the RLGM

h. Designed the Synchronizer and framing P.C.B.'s on a single P.C.B. and made it interchangeable with other Framing Synchronizer P.C.B.'s in other units

i. Designed the Clock and Timing P.C.B. so that it is interchangeable with other GTE Sylvania units

j. Other mechanical design approaches are discussed in paragraph 15.4 of this volume.

7.2.2 Detailed Electrical Design for the RMC

A detailed block diagram of the RMC is shown in Figure 7-1. The RMC multiplexes an input loop group from either a Remote Loop Group multiplexer (RLGM) or another RMC and/or up to eight digital subscriber loops into a single digital output group. The RMC design uses two separate MUX/DEMUX and Group Framing P.C.B.'s, one for the input group and one from the output group. In effect, the RMC takes the incoming group and breaks the group apart into its

separate data streams. The separated loop data from the input group is then combined with the eight digital subscribers and the output (output group) overhead channel and re-multiplexed for transmission to the output group channel. Frame synchronization is maintained with each group by separate framing/synchronizer units.

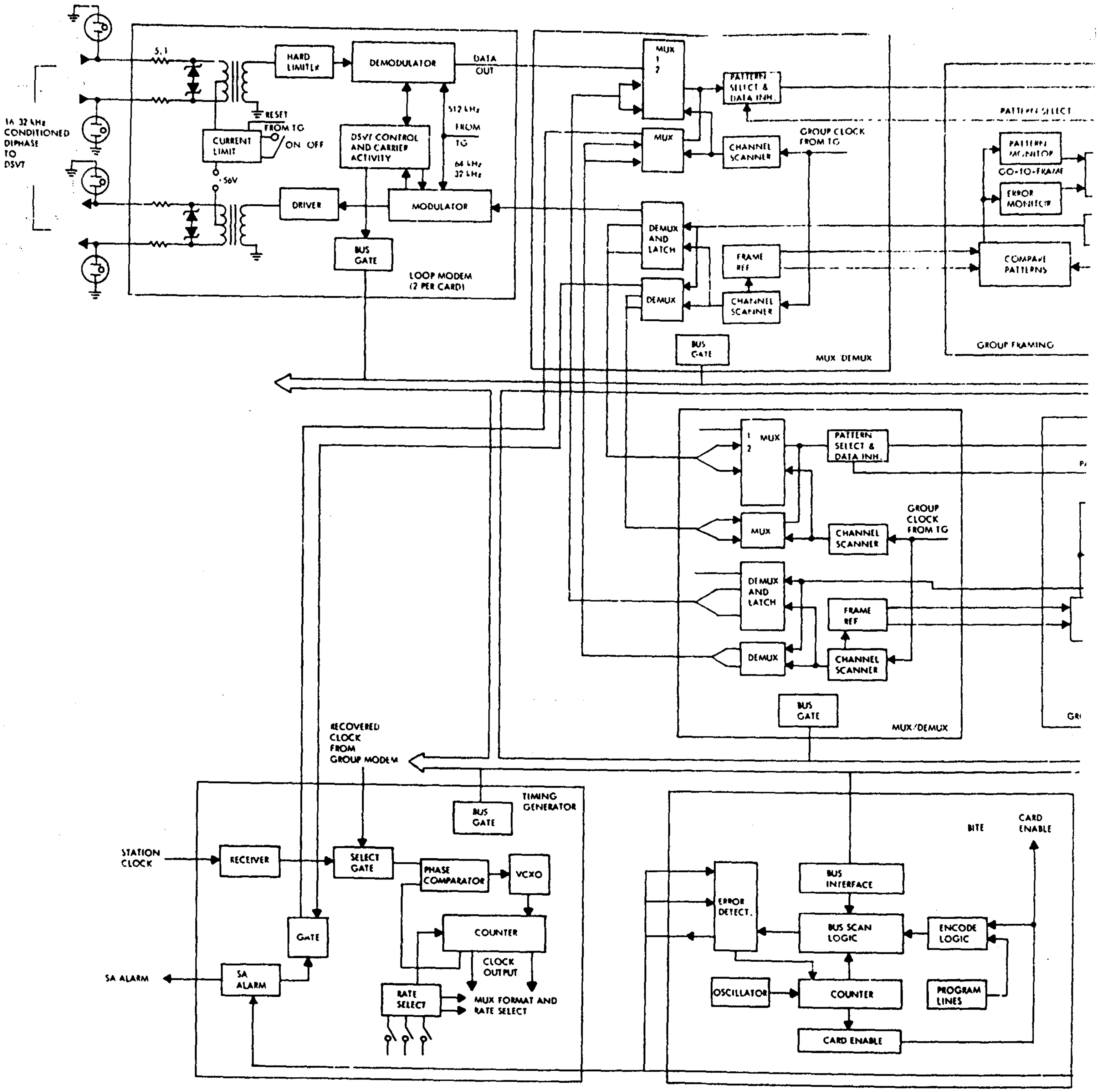
The RMC contains eight (8) conditioned diphase loop modems. Two modems are packaged on a single P.C.B.

The loop modems accept baseband digital loop signals from the output group MUX DEMUX P.C.B. and modulate/demodulate the loop data for transmission to digital voice subscriber terminals via telephone (WF-16) cable. The modems also provide phantom loop power over this same cable to power the DSVT operating in a common battery mode. A switch is provided on each loop modem to control the power (on/off) to each DSVT. EMP devices required for first level protection are mounted on the RMC's signal entry panel for each loop. Second level EMP protection circuits are located on each loop modem.

The Loop Modem NRZ baseband data is passed to the MUX/DEMUX card where it is multiplexed with the overhead channel containing the SYSCON subchannel. The resulting bit interlaced data stream is sent to the output Group Framing Unit where the data is gated to the output group data interface under control of the synchronizer section of the Group Framing Unit. The output group baseband data stream is connected to the Group Modem. The Group Modem converts the baseband data to conditioned diphase for transmission on the RMC output group.

The input data of the output group is demodulated by the Group Modem producing a baseband signal compatible with C-MOS logic. The group Modem also performs the clock recovery function which is required to lock the RMC's Internal Timing Generator to the incoming data stream when station clock is not used.

The baseband data is then connected to the frame regenerator portion of the output Group Framing Unit. The frame regenerator is a counter whose output (frame pattern) is aligned in phase with the incoming frame pattern in the



1A 32 kHz
CONDITIONED
DIPHASE
TO
DSVT
HARD LIMITER
DEMODULATOR
DATA OUT
RESET
FROM TG
CURRENT LIMIT
ON OFF
DSVT CONTROL AND CARRIER ACTIVITY
512 kHz
FROM TG
64 kHz
32 kHz
-56V
DRIVER
MODULATOR
BUS GATE
LOOP MODEM
(2 PER CARD)
MUX 1 2
MUX
PATTERN SELECT & DATA INH.
CHANNEL SCANNER
GROUP CLOCK FROM TG
DEMUX AND LATCH
FRAME REF
DEMUX
CHANNEL SCANNER
BUS GATE
MUX DEMUX
PATTERN SELECT
PATTERN MONITOR
GO-TO-FRAME
ERROR MONITOR
COMPARE PATTERNS
GROUP FRAMING
MUX/DEMUX
RECOVERED CLOCK FROM GROUP MODEM
TIMING GENERATOR
BUS GATE
STATION CLOCK
RECEIVER
SELECT GATE
PHASE COMPARATOR
VCXO
COUNTER
GATE
CLOCK OUTPUT
SA ALARM
RATE SELECT
MUX FORMAT AND RATE SELECT
BITE
CARD ENABLE
ERROR DETECT.
BUS INTERFACE
BUS SCAN LOGIC
ENCODE LOGIC
OSCILLATOR
COUNTER
PROGRAM LINES
CARD ENABLE

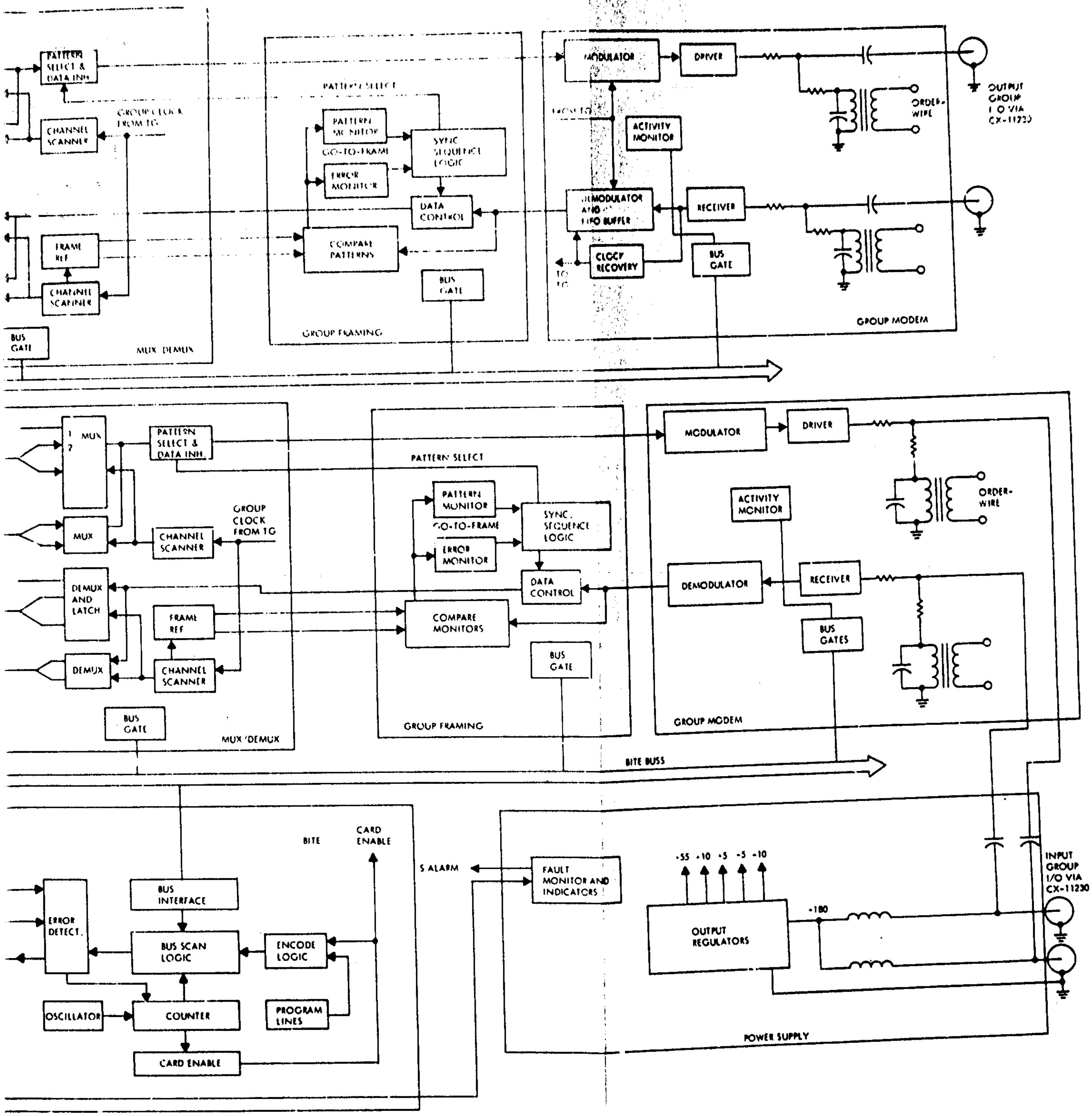


Figure 7-1. RMC Block Diagram

2

MUX/DEMUX circuitry. The demultiplexed data channels are buffered, and applied to each loop via the Loop Modems. Binding post terminals mounted on the RMC's signal entry panel are used to connect each loop with the DSVT's.

An analog voice orderwire channel is provided on each Group Modem in the RMC for set up and maintenance of cable systems utilizing CX-11230 Cable. The appropriate filters required to separate the orderwire analog signal from the data are located on each group modem P.C.B. Two external connectors (one for the high group and one for the low group) are provided on the RMC's signal entry panel for connection to the Cable Orderwire Unit (COU).

The Timing Generator locks an internal oscillator to either an external clock or to the high groups incoming recovered clock. A toggle switch located on the high Group Modem P.C.B. is used to select this function. Toggle switches located on the Timing Generator P.C.B. are used to program the proper output clock rates, the switch outputs are also used to program the MUX/DEMUX card.

Capability of looping back the SYSCON subchannel of the high group is provided on the Timing Generator P.C.B. The loop-back function is interrupted and all ZERO's are inserted at the input to the high group sub-channel multiplexer when a Summary BITE error (SA) has been detected.

The BITE card monitors key signal status on each P.C.B. within the RMC. These signals are transmitted to the BITE P.C.B. over a sixteen (16) bit buss. The BITE P.C.B. sequentially addresses each P.C.B. within the unit and determines whether all the "key" signals are present. If not, a one second delay is started and the signals tested again. If after the one second delay, the fault persists, a summary error flag is raised. This flag causes the S and the SA (depending upon the fault) alarm's to be energized. An LED located on the defective P.C.B. will then be illuminated along with the Summary Error indicator located on the front panel of the power supply. In the event that the BITE has detected a fault which could be caused by an external error (interface unit), the LED located on the BITE P.C.B. will illuminate. The fault LED located on the BITE P.C.B. is used to indicate external errors only.

The RMC power supply operates from +28 VDC, 120 Volt AC, 50 to 400 HZ single phase power. The power supply outputs are ± 10 VDC, ± 5 VDC, + 55 VDC and + 180 VDC. The 5 and 10 VDC voltages are used internally to power the RMC P.C.B.'s. The +55 Volt output is used for powering the DSVT's via phantom loops. The +180 volt ouput is used to remotely power an RLGM. The power is coupled to the input group's CX-11230 cable through de-coupling capacitors and chokes located in the power supply.

The Power Supply contains fault monitoring circuits which monitor the status of each output voltage. When an out-of-tolerance indication is detected, the Power-out-of Tolerance and Summary Fault indicators are illuminated.

7.2.3 Interface Description

The Remote Multiplexer Combiner (RMC) is a standalone unit designed for field portable, exposed use. The width of the RMC case is small enough to allow mounting to MIL-STD-189 racks within shelters or vans. Appropriate mounting brackets (not supplied) are required for this type of installation.

The RMC is designed to multiplex an input digital time division multiplexed loop group from a Remote Loop Group Multiplexer (RLGM), another RMC, and or up to eight digital subscriber loops into a single output digital time division multiplexed loop group.

The RMC interface requirement is summarized in Table 7-2 and described in the following sections.

7.2.3.1 Loop Interface (32 binding posts)

Loop interfaces are provided to connect to eight full duplex digital loops. Each loop interface consists of transmit loop data and receive loop data. The signals are conditioned diphase modulated signals. The signal rates are conditioned diphase modulated signals. The signal rates are 16 kb/s or 32 kb/s. The signal lines are balanced. Fifty-five volts maximum (measured at the RMC terminals) is provided in each loop for powering each Digital Secure Voice Terminal (DSVT) terminated on the loop side of the RMC.

TABLE 7-2. RMC INTERFACE SPECIFICATION SUMMARY

Connector	Function	Signal Rate/ Frequency	Signal/Line Characteristics	Type of Cable Connection Required	Number of Wires in Connector
32 Binding Posts	• Transmit and receive Loop data - channels 1 through 8	16 or 32 kb/s	Conditioned Diphase, Balanced	16 PR (Field Wire-WF-16)	-
J1	• Low group transmit data • Low group receive data	72, 128, 144 kb/s for loop rate of 16 kb/s or 144, 256, 288 kb/s for loop rate of 32 kb/s	Conditioned Diphase, Unbalanced	UG-1837 (Dual coax)	2 Coax
J2	• High group transmit data • Low group receive data	128, 144, 256, 288 kb/s for loop rate of 16 kb/s or 256, 288, 512, 576 kb/s for loop rate of 32 kb/s	Conditioned Diphase, Unbalanced	UG-1837 (Dual coax)	2 Coax
J3	• Station clock	At high group rate	NRZ, Balanced	1 shielded twisted pair	3
J4	• Alarm SA	Contact Closure	-	2 pairs with overall shield	5
	• Alarm S	Contact Closure	-		
J5	• Prime power	AC 50, 60 or 400 Hz or DC +28 volts	-	3 conductors	3
J6	LO GR Orderwire In LO GR Orderwire Out	300 - 3500 Hz Analog	Balanced 600Ω	2 pair with shield	5
J7	HI GR Orderwire In HI GR Orderwire Out	300 - 3500 Hz Analog	Balanced 600Ω	2 pair with shield	5

Two watts maximum is supplied by the RMC for each DSVT connection. Connections on the loop side are made with WF-16 field wire. Sieman's gas-filled surge arrestors are used on first level EMP protection. One Sieman's arrestor is placed across each binding post terminal, the binding post is permanently mounted to the Signal Entry Panel (SEP) of the case. The connections from the SEP binding posts to the P. C. B. nest are direct wiring. Refer to RMC mechanical layout in Section 15.4.2 of this volume.

7.2.3.2 Low Group Interface (J1)

The input group interface is a full duplex digital group which connects to an RLGM or another RMC. The low input group interface consists of (1) transmit group data and (2) receive group data. The signals are conditioned diphase modulated signals. The signal bit rates are 144 kb/s, 256 kb/s, or 288 kb/s when the channel bit rate is 32 kb/s. The signal bit rates are 72 kb/s, 128 kb/s or 144 kb/s when the channel bit rate is 16 kb/s. The signal lines are unbalanced. DC power is supplied over this interface to power a Remote Loop Group Multiplexer (RLGM).

Connection to the low Input Group Interface is by CX-11230 Coax cable.

7.2.3.3 High (Output) Group Interface (J2)

The output group interface interfaces with a full duplex digital group which connects to an AN/TTC-39 switch, AN/TSQ-111 Communications Nodal Control Element, Group Modem or another Remote Multiplexer Combiner (Low Group Interface or High Group Interface). The high group interface consists of (1) transmit group data and (2) receive group data. The signals are conditioned diphase modulated signals. The signal bit rates are 256 kb/s, 288 kb/s, 512 kb/s, or 576 kb/s when the channel bit rate is 32 kb/s. The signal bit rates are 128 kb/s, 144 kb/s, 256 kb/s or 288 kb/s when the channel bit rate is 16 kb/s. The signal lines are unbalanced. Connection to the High Group Interface is by CX-11230 coax cable.

7.2.3.4 Station Clock (J3)

The station clock is a square wave with a frequency equal to the output group bit rate. The Station Clock line is balanced.

7.2.3.5 ALARM Signals (J4)

A connector is provided to carry a contact closure for the S ALARM and the SA ALARM outputs. The alarm conditions are a contact closure.

7.2.3.6 Prime Power (J5)

A common connector is provided to accept the prime power to the RMC. The input power is 120 VAC $\pm$ 10%, 50 to 400 Hz or +28 $\binom{+4}{-6}$ volts dc. The power cable must have an overall cable shield.

7.2.3.7 Orderwire (J6 and J7)

The Low Group orderwire on J6 is a 600 ohm balanced input full duplex analog voice frequency circuit. The High Group orderwire on J7 is identical.

7.3 DETAIL ELECTRICAL DESIGN

7.3.1 Introduction

As was previously explained, logic P.C.B.'s were designed which are used in more than one unit. This is possible since there are many functions which are similar in these units. Consequently, it was decided to design these cards with emphasis on commonality. Variations in specific unit functions are taken care of by either toggle switches mounted on the P.C.B. or by back-plane wiring. For purposes of this technical report, we will describe the card in detail in the first section covering that material. References will then be made to this paragraph in subsequent sections.

7.3.2 Loop Modem

The Loop Modem is a WF-16 field wire carrier terminal which provides full duplex transmission of binary data signals at 32/16 kb/s between DSVT terminals and the RMC.

Figure 7-2 illustrates the block diagram of the diphase modulator. Refer to section 3.3.5.1 for the description.

Figure 7-3 illustrates the block diagram of the diphase demodulator. Refer to section 3.3.5.2 for the description.

7.3.3 Mux/Demux (RMC)

The multiplexing and demultiplexing function in the RMC is achieved through the use of two identical Mux/Demux cards. One of these cards is used on the Input group data stream and one of these cards is used on the combined Output group data stream. The 32 kb/s channel sides of the two Mux/Demux cards will be interconnected so as to achieve the Group Output time sequencing of channels. Figure 7-4, RMC Formats, shows the rates for the Input Group, the Output Group and the loop bit rates which the Mux/Demus operates on. Included on that figure is the number of channels for each of the data I/O ports. Figure 7-5 shows how and RLGM input group will be connected to the RMC output group, Figure 7-6 shows how an RMC will be connected to another RMC through the high and low multiplexers. The multiplexers shown are full duplex. however the MUX/DEMUX function shown for each group is contained on identical P.C.B.'s.

For a detailed discussion of how the multiplexing scheme is implemented, refer to paragraph 3.3.2.

The Mux/Demux cards are programmable by the encoded selector switches from the timing card. They select the number of output channels, either 8, 9, 16 or 18, and one of four output modes (1, 2, 3, 4) as shown in Figure 7-7. In addition, the counter is preset such that the group clock is divided by 8, 9, 16, 18 which provide the positions of the overhead channel.

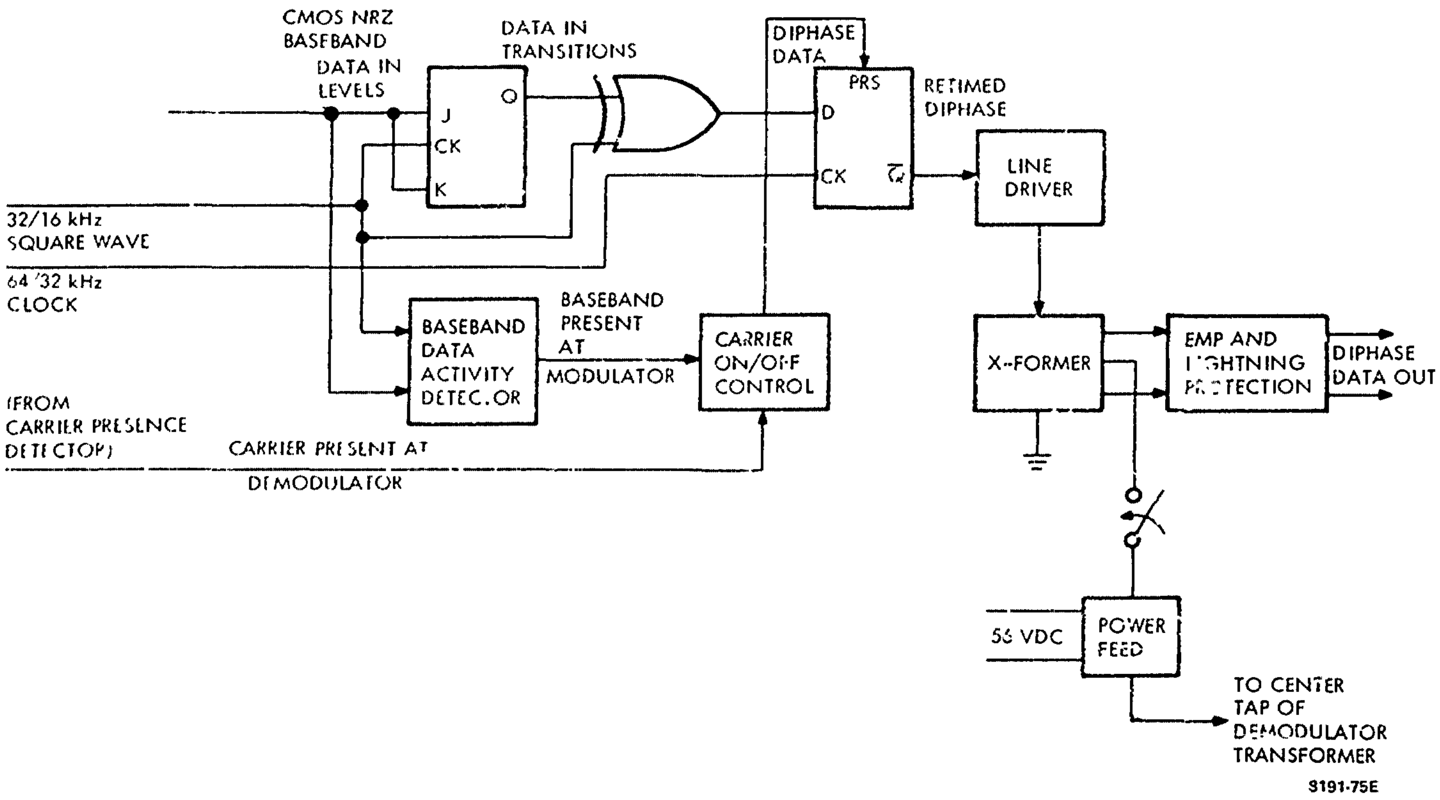


Figure 7-2. Loop Modem Modulator Section

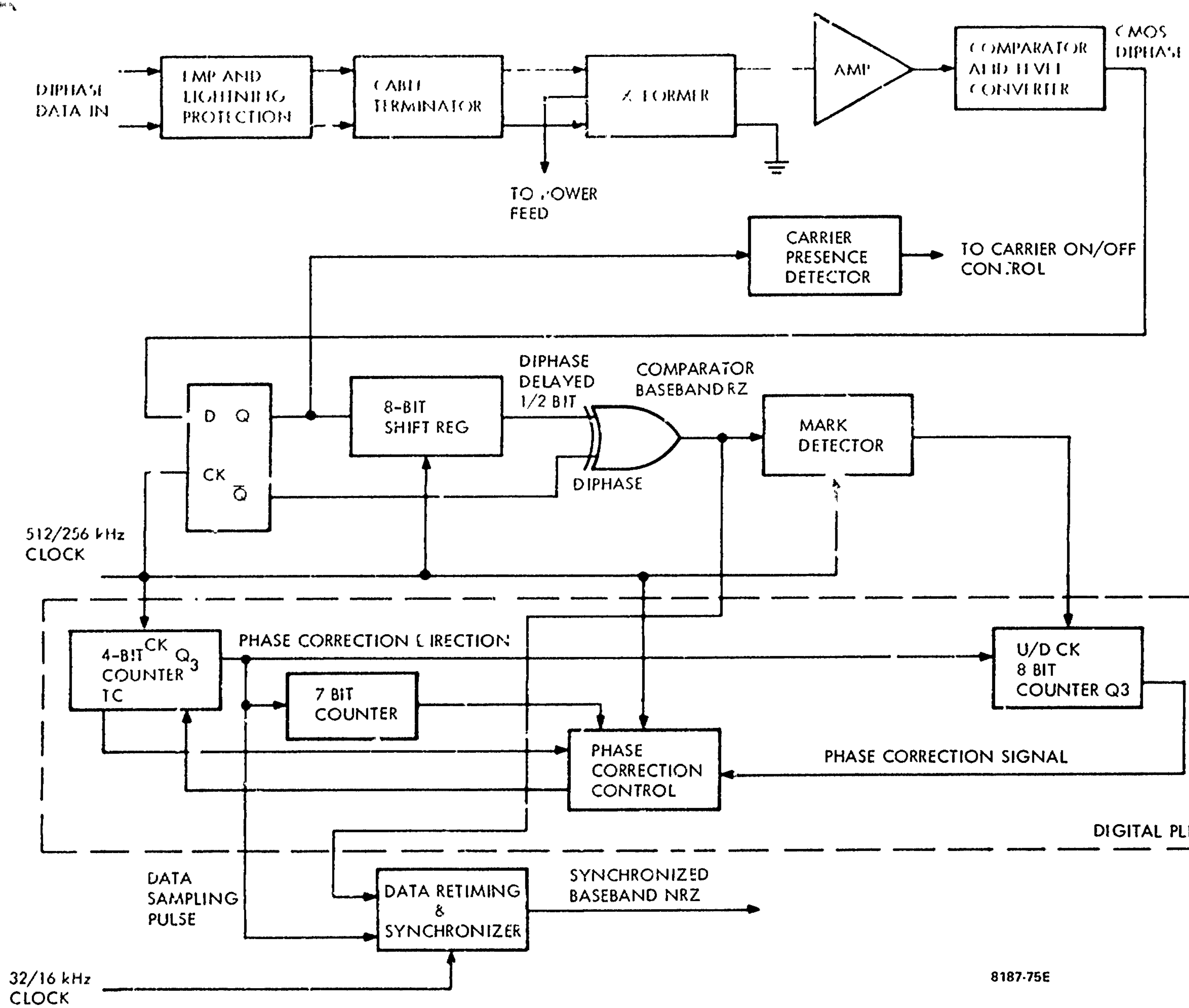


Figure 7-3. Loop Modem Demodulator Section

INPUT SIDE				OUTPUT SIDE	
LOOP		INPUT GROUP		OUTPUT GROUP	
NUMBER OF LOOPS	LOOP BIT RATE	NUMBER OF CHANNELS	INPUT GROUP BIT RATE	NUMBER OF CHANNELS	OUTPUT GROUP BIT RATE
3	32 kb/s	4 1/2	144 kb/s	8	256 kb/s
4	32	4 1/2	144	9	288
8	32	8	256	16	512
8	32	9	288	18	576
7	32	not used	---	8	256
8	32	not used	---	9	288
3	16	4 1/2	72	8	128
4	16	4 1/2	72	9	144
8	16	8	128	16	256
8	16	9	144	18	288
7	16	not used	---	8	128
8	16	not used	---	9	144

8155-75E

Figure 7-4. RMC Formats

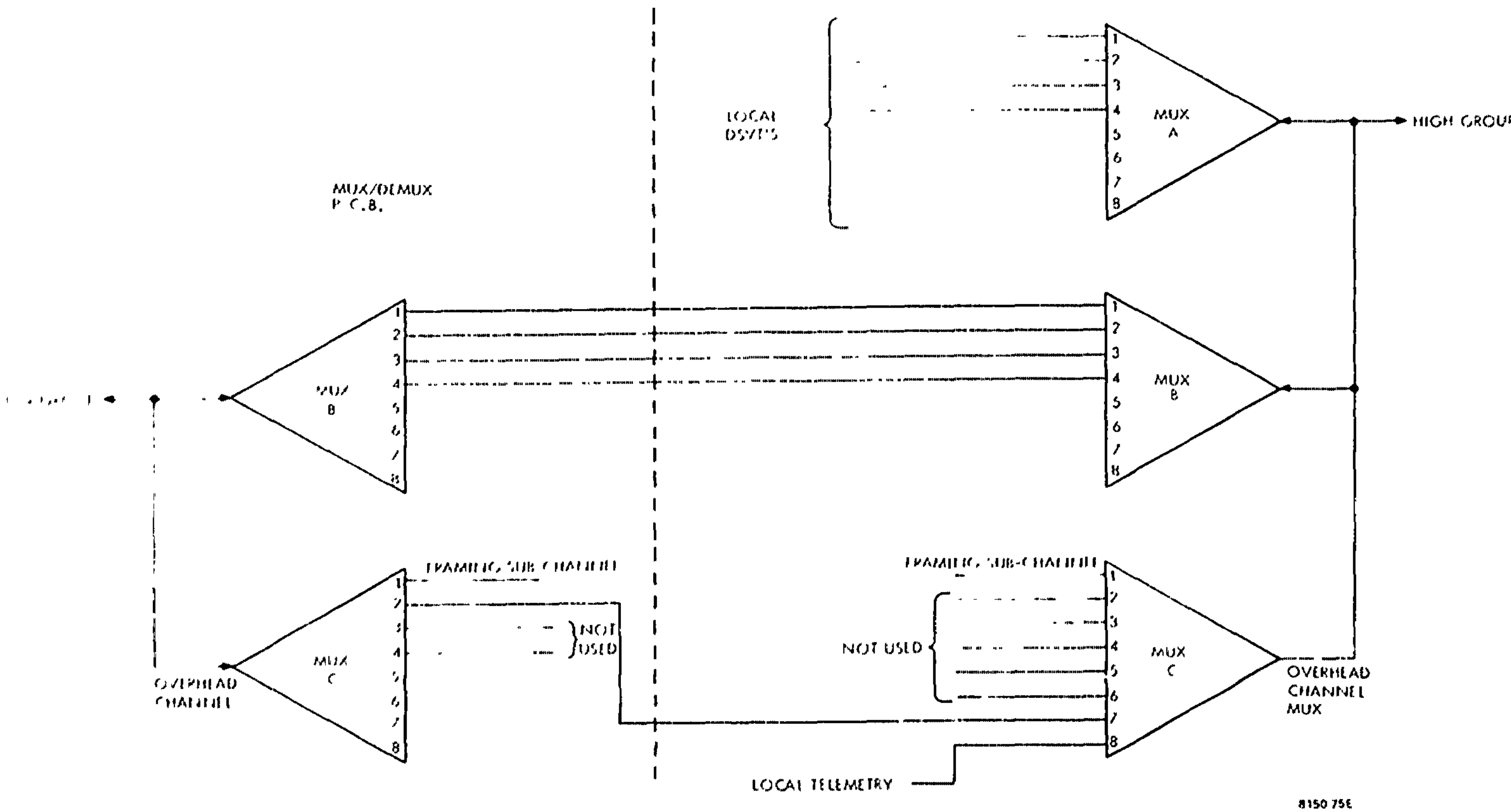


Figure 7-5. RLGM to RMC MUX/DEMUX Connections

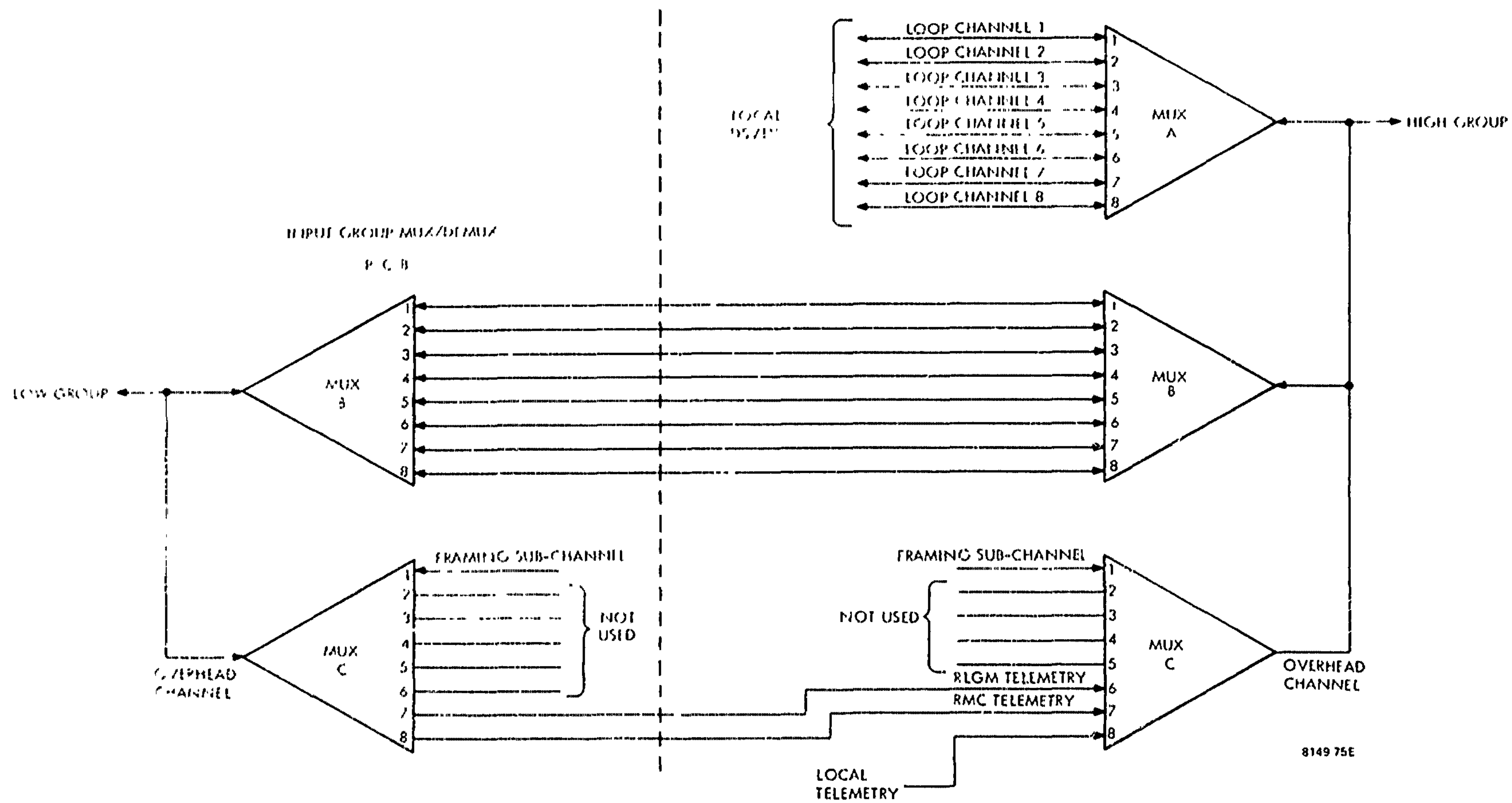


Figure 7-6. RMC to RMC MUX/DEMUX Connection Diagram

MODE	GROUP INPUT	LOOP INPUT	SPARE	TOTAL NUMBER CHANNELS	OUTPUT PATTERN
1	0	7	0	8	0 A1 A2 A3 A4 A5 A6 A7 0
1	0	8	0	9	0 A1 A2 A3 A4 A5 A6 A7 A8 0
2	4	4	0	9	0 A1 B1 A2 B2 A3 B3 A4 B4 0
2	7	8	0	16	0 A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7 A8 0
3	4	3	0	8	0 B1 A1 B2 A2 B3 A3 B4 0
4	8	8	1	18	0 SP A1 B1 A2 B2 A3 B3 A4 B4 A5 B5 A6 B6 A7 B7 A8 B8 0

A = LOOP INPUTS

B = GROUP INPUTS

8156-75E

Figure 7-7. RMC Output Configurations

The Mux/Demux card on the input group side of the RMC is set to 4-1/2, 8, and 9 channels and is always set to mode 1. (Also see Figure 7-8, Input Group Formats.)

7.3.3.1 Multiplexing of the Input Group and Loop Inputs

In order to combine a 4-1/2, 8, or 9 channel input group with either the 3, 4, 7 or 8 local loops to produce a combined group output, it is necessary to break the group input apart into separate data streams. By doing this, the input and output groups can be constructed with their associated data channels appearing at the proper time sequences.

The multiplexer on the Output Group side contains three 8-bit multiplexers, one for the loop inputs (multiplexer A), one for the Demux Group Channel inputs (multiplexer B) and one for the combination of the Demuxed I/O Group overhead subchannels and the local or external Telemetry Channel (card multiplexer C).

On this Group Output side, the Subchannel Mux time (multiplexer C) time multiplexes a 4 kb/s frame pattern and subchannels into an overhead channel. The frame pattern selection is determined by the Pattern Control signal from the synchronizer card. One subchannel is used for telemetry from the 4-1/2 channel size group or up to three subchannels will be used for telemetry for the larger size groups (Figure 7-9, MRC Overhead Channel Formats).

The 7th overhead subchannel is utilized for local telemetry from either a 2 kb/s external input or the 150 b/s output from the telemetry generator. A card edge selector switch determines which telemetry signal will be multiplexed.

The 6th overhead subchannel is utilized for the telemetry from the connected RLGM or RMC and the 5th overhead subchannel will be utilized for the RLGM telemetry via the connected RMC.

The Output Control circuitry can inhibit the data channels to the Output Group or to the Input Group from the mux upon command from the synchronizer card. The Data Control signal provides the control to either output data or all 0's in the data channel time slots. In either case, the frame pattern is passed

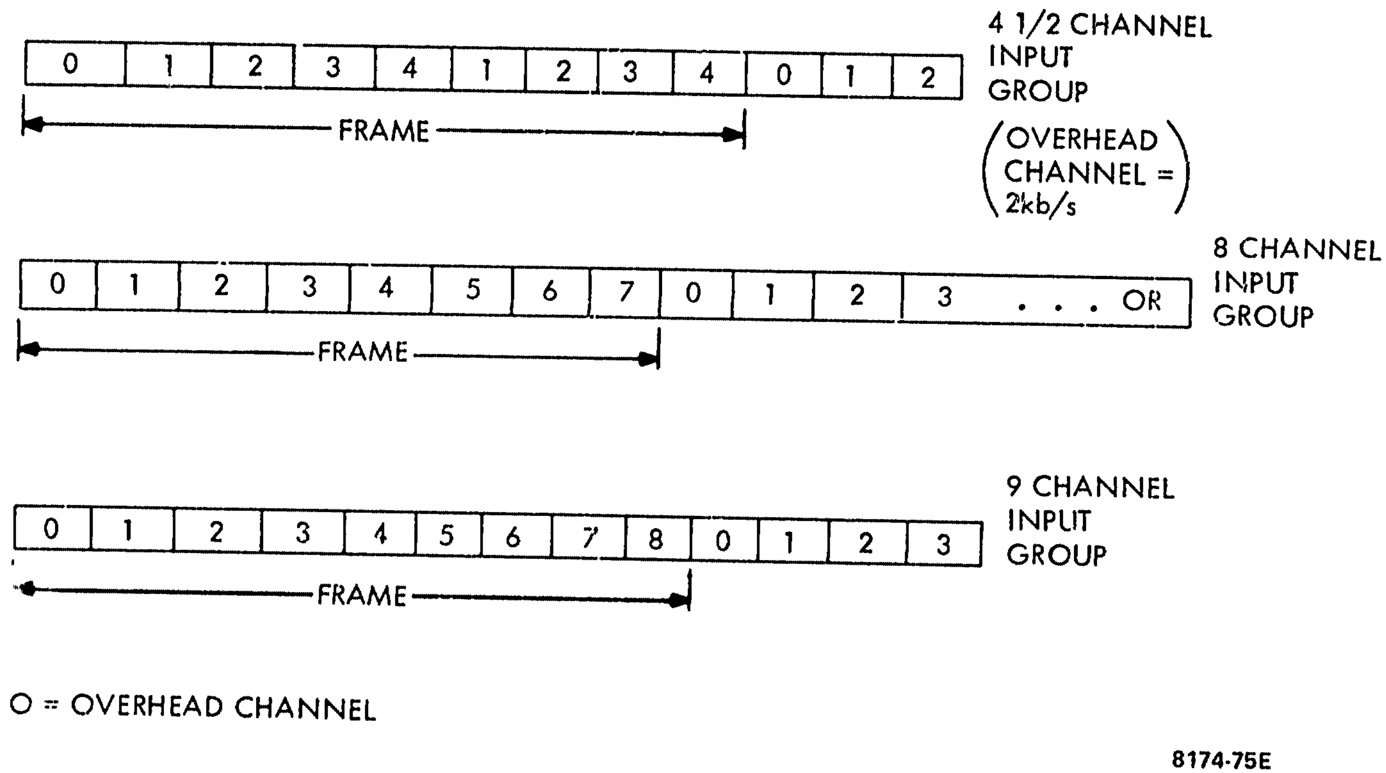


Figure 7-8. Input Group Formats

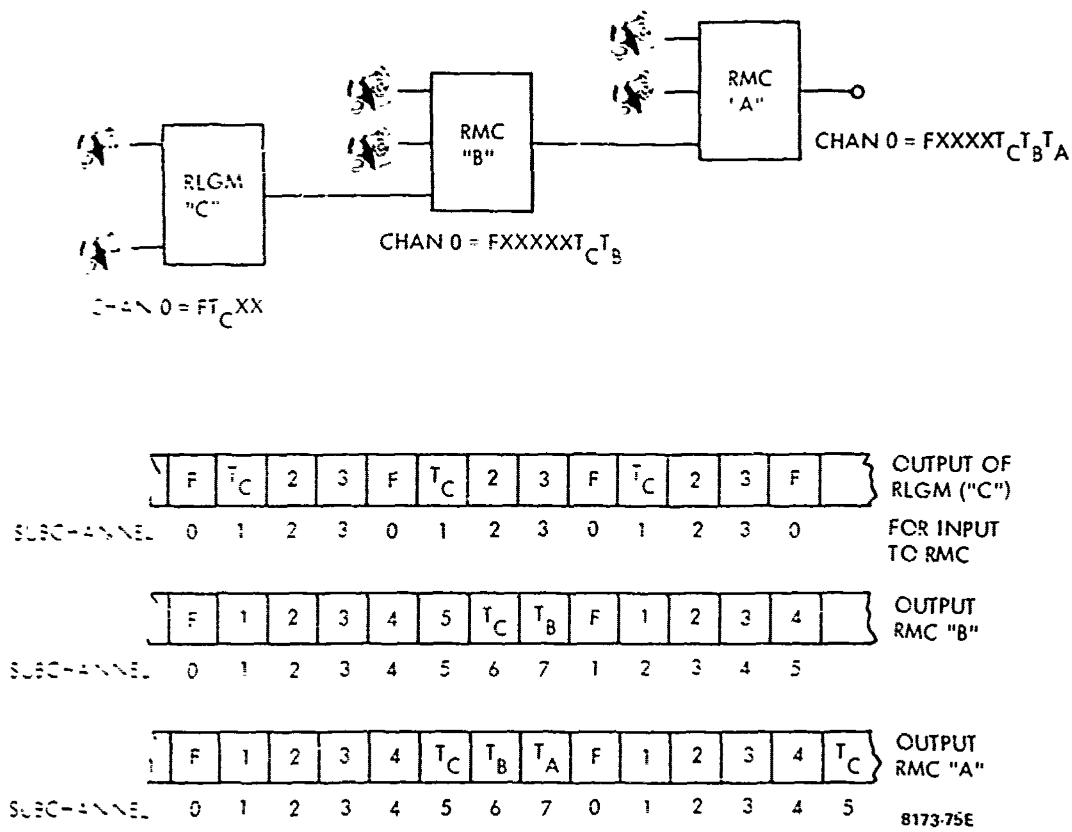


Figure 7-9. RMC Overhead Channel Formats

through unaltered. Three possibilities exist (see Figures 7-10 through 7-12).

Case I - The Output Group side is out of frame sync but the Input Group side is in frame sync.

In this case, 0's will be sent on the data channels to the output of the Output Group side. Data received from the Output Group side will be forced to be all 1's and distributed to the respective channel destinations.

Case II - The Output Group is in frame sync, but the Input Group is not in frame sync.

The data received from the Input Group will be forced to be all 1's and loop data will pass through unaltered. Data sent to the Input Group side will be forced to be all 0's (except for the frame channel). Therefore, communications with the telephone data will continue with the Output Group side.

Case III - Both Input Group and Output Group data are out of frame sync.

The data to the Group Outputs will be 0's (except for the frame unit) and the data to the loop channels will be 1's.

7.3.3.2 Data from Output Group Side

The programmable channel demux receives reframed data and a frame reference signal from the framing unit and demultiplexes the group into loop channels, group channels, and overhead subchannels in a preselected manner similar to the method used for multiplexing. Subchannel 7 is routed to an external output and subchannels 5 and 6, as well as the input group channels, are remultiplexed and transmitted to the connected RMC or RLGM on the input group side.

7.3.4 RMC: Framing/Synchronizer Unit

The Framing Synchronizer card used in the RMC is identical to the card used in the LGM (see section 3.3.3) with the following exceptions: the RMC does not provide a "squelch" input for inhibiting frame search and does not include provisions for a TED. The manual switch located on the card edge "TED equipped non-equipped" is nonfunctional; the proper switch position is hardwired on the back plane.

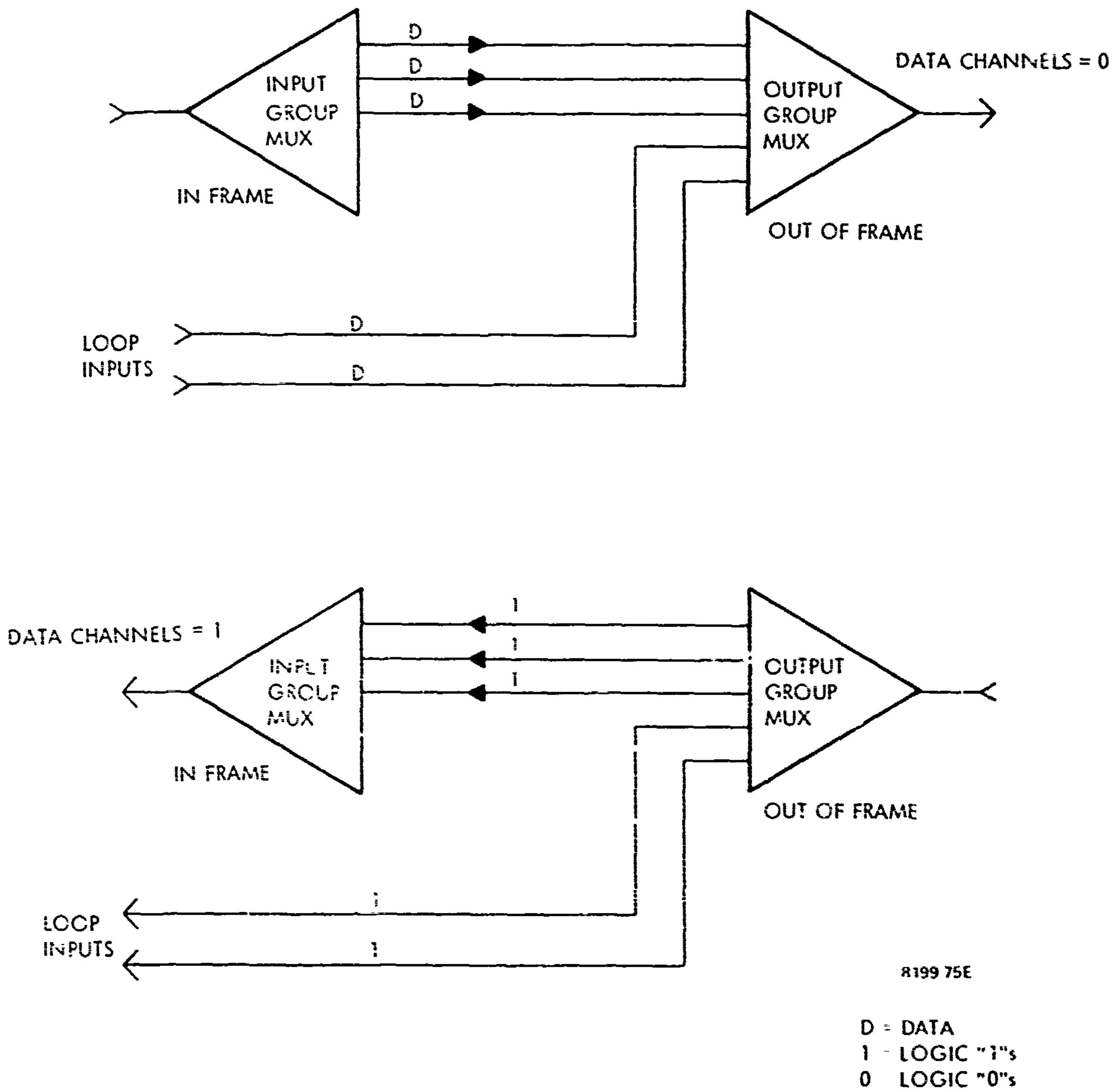
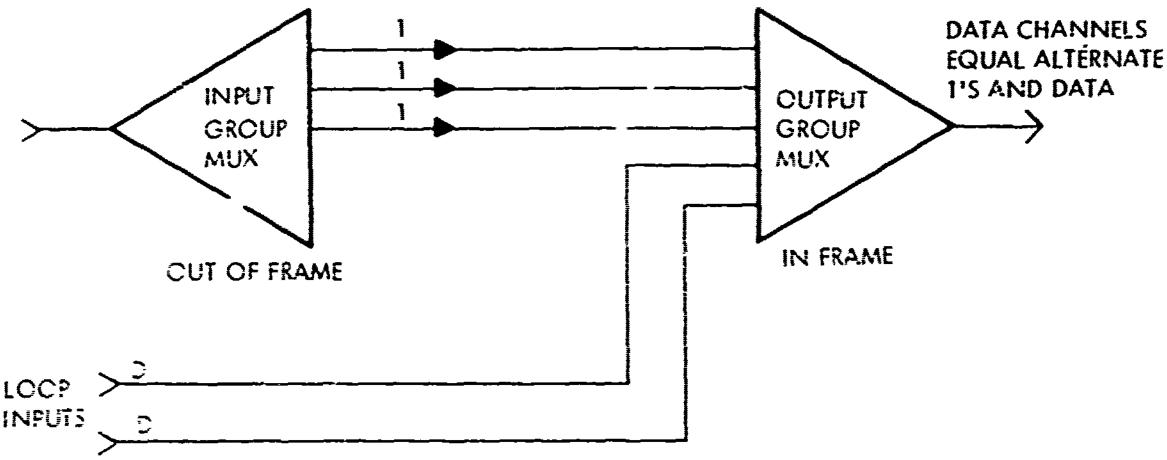


Figure 7-10. Case 1



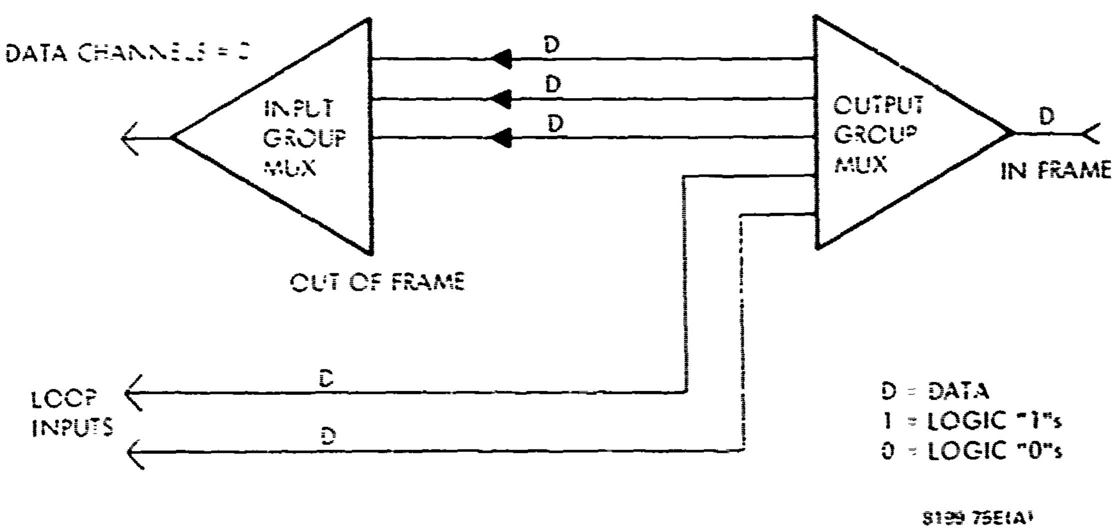


Figure 7-11. Case II

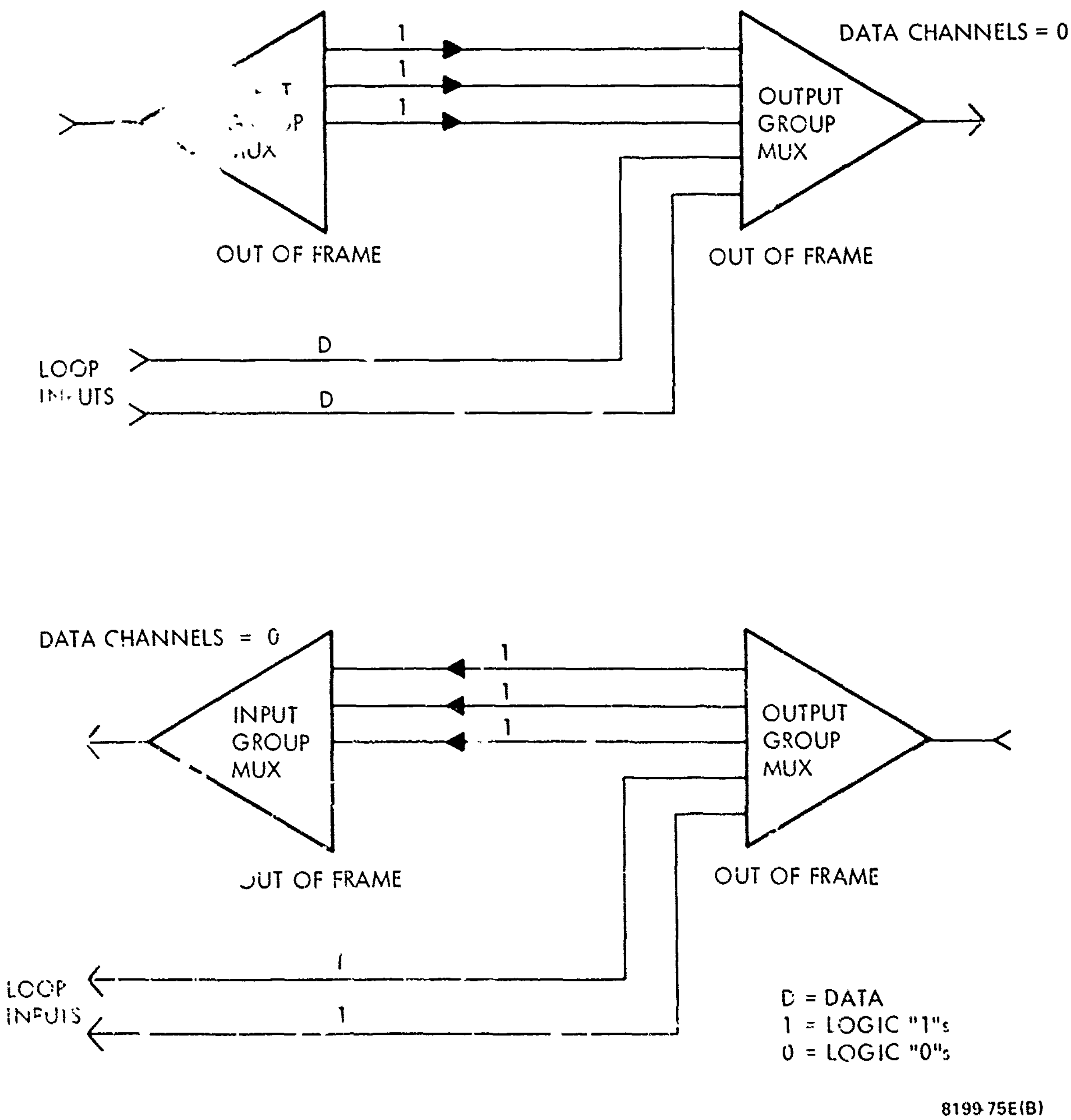


Figure 7-12. Case III

A block diagram of the framing portion of the card is shown in Figure 7-13 and the synchronizer in Figure 7-14.

7.3.5 Group Modem - RMC

The Group Modem (GM) provides full duplex transmission of synchronous binary data signals at the group level. The data is transmitted via conditioned diphase modulated carrier over CX-11230 ( )/G coaxial cable. Figure 7-15 is a block diagram of the modulator, refer to Section 5.3.5.1 for details.

Figure 7-16 is a block diagram of the demodulator, refer to Section 5.3.5.2 for details.

7.3.6 Clock and Timing for the RMC

The same Timing Generator card is used in the LGM, RLGM, and RMC. Various combinations of rates are required in the different units; the rate combinations are shown in Table 7-3. Rate select switches S1, S2 and S3 select the proper clock outputs. A strap on the card selects the rate family based on 16 or 32 kb/s channel rates. The clock and timing circuitry is shown in Figure 7-17. A phase-locked loop is employed to lock an internal voltage controlled crystal oscillator to either an external station clock or the recovered group clock from the group modem circuit.

The Timing Generator provides 12 clock pulse outputs, a loss-of-lock output level, and 11 program lines as shown in Figure 7-17. One card is used in the RMC. LGM, and RLGM.

All clock outputs are phase locked to the incoming station clock, which has a range of 576 kHz to 72 kHz, depending upon the unit in which it is used as shown in Table 7-3. The input station clock is buffered by a line receiver for a balanced input.

Three toggle switches (S1, S2, S3) serve as control inputs. A forth input (a strap) selects the loop rate of 32 kHz or 16 kHz. The three control switch levels are decoded into 11 output lines which program the MUX/DEMUX board as used in the RMC and LGM. Table 7-4 is a lising of OUTPUTS A thru K and CONTROL

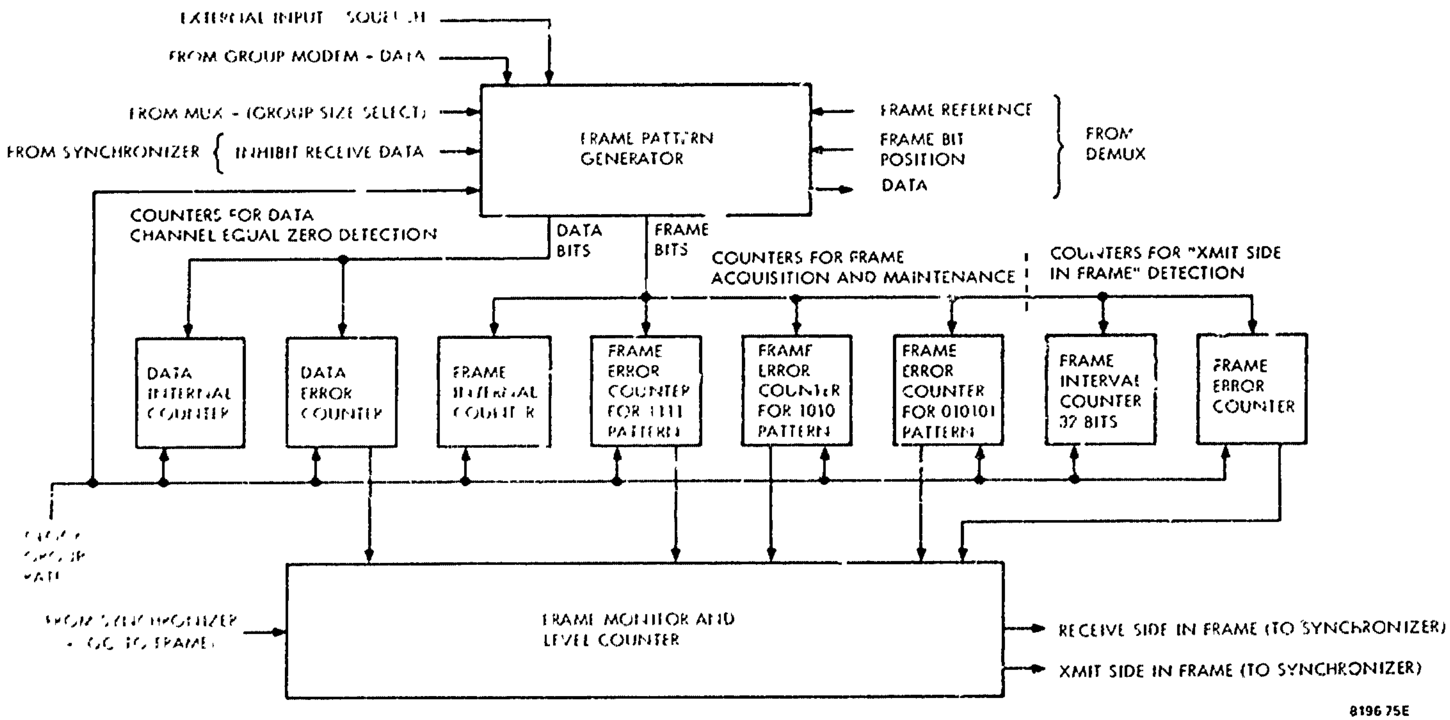


Figure 7-13. Framing Block Diagram

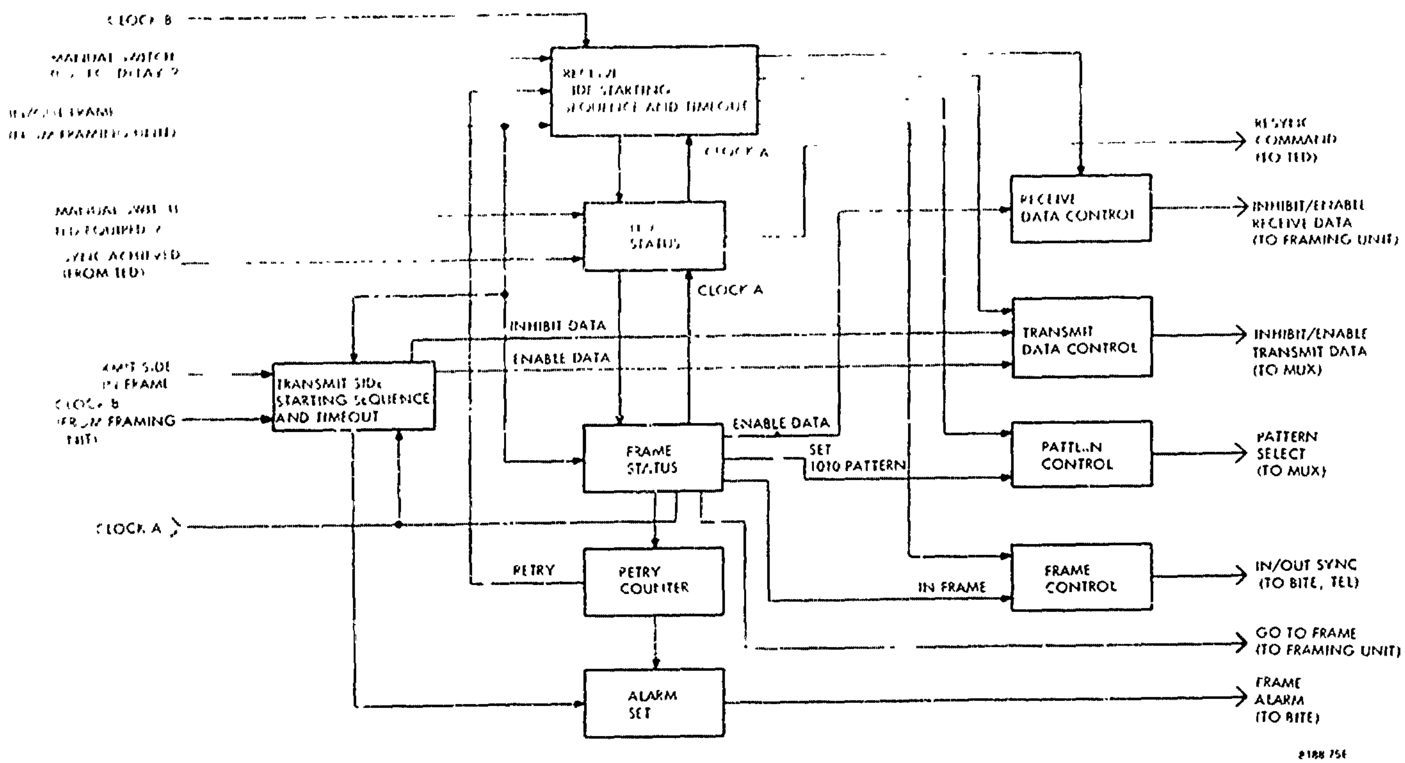


Figure 7-14. Frame Synchronizer Block Diagram

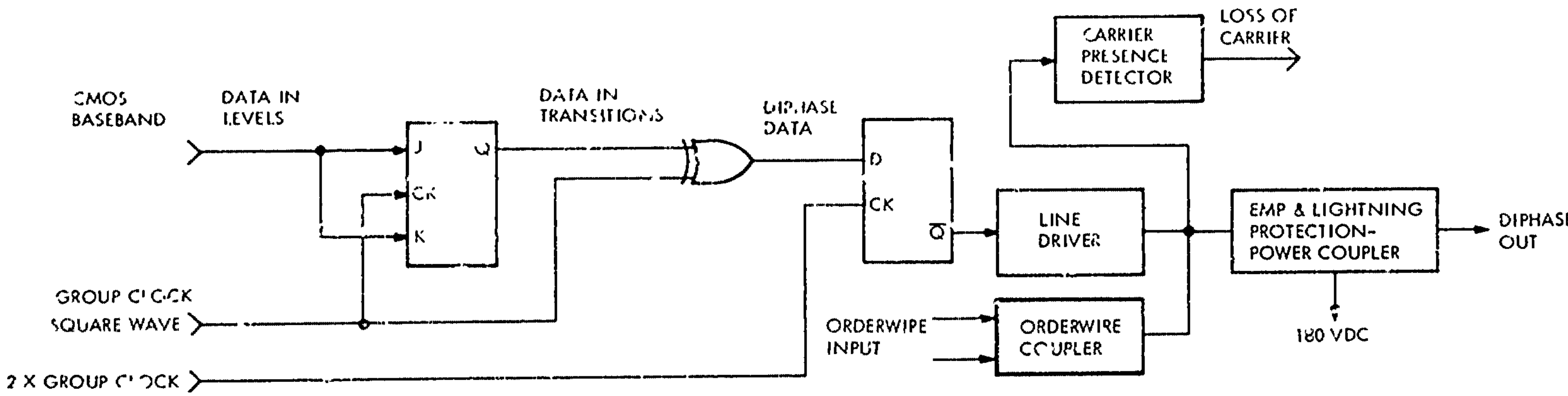


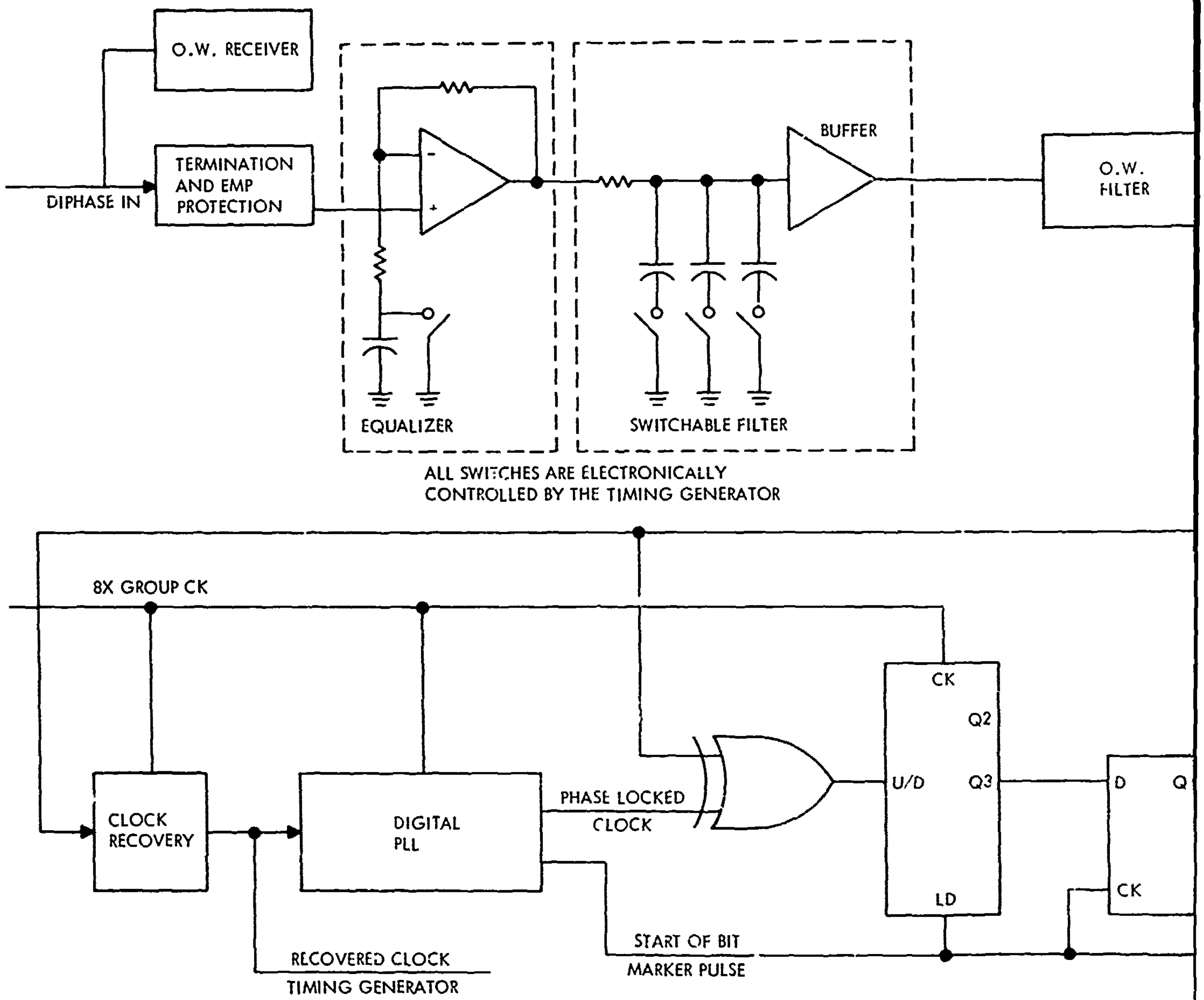
Figure 7-15. Group Modem Modulator Section

TABLE 7-3. TIMING GENERATOR OUTPUTS

RLGM Configuration	-	4 1/2 Chan	-	-	-	-
LGM Configuration	8 Chan	9 Chan	-	-	16 Chan	18 Chan
RMC Configuration Input	4 1/2 Chan	4 1/2 Chan	-	-	8 Chan	9 Chan
RMC Configuration Output	8 Chan	9 Chan	8 Chan	9 Chan	16 Chan	18 Chan
Switch 1	1	1	0	0	1	1
Switch 2	0	1	0	1	0	1
Switch 3	1	0	1	0	0	1
CLOCKS						
* Station Clock, Recovered Clock, or Data Clock Input	256	288	256	288	512	576
* Output Group	256	288	256	288	512	576
* 2X Output Group	512	576	512	576	1024	1152
* 8X Output Group	2048	2304	2048	2304	4096	4608
* Input Group	144	144	144	144	256	288
* 2X Input Group	288	288	288	288	512	576
* 8X Input Group	1152	1152	1152	1152	2048	2304
* Loop Modem Clock 1	512	512	512	512	512	512
* Loop Modem Clock 2	64	64	64	64	64	64
* Loop Modem Clock 3	32	32	32	32	32	32
Group Framing Clock	32	32	32	32	32	32
Telemetry Clock	2	2	2	2	2	2
Timeout Clock	0.15	0.15	0.15	0.15	0.15	0.15

NOTES: 1. * Rates halve when 16 kb/s DSVT's are used

2. All rates are in KHz


O.W. RECEIVER
TERMINATION AND EMP PROTECTION
DIPHASE IN
BUFFER
O.W. FILTER
EQUALIZER
SWITCHABLE FILTER
ALL SWITCHES ARE ELECTRONICALLY CONTROLLED BY THE TIMING GENERATOR
8X GROUP CK
CLOCK RECOVERY
DIGITAL PLL
PHASE LOCKED CLOCK
CK
Q2
U/D
Q3
LD
D
Q
CK
START OF BIT MARKER PULSE
RECOVERED CLOCK
TIMING GENERATOR

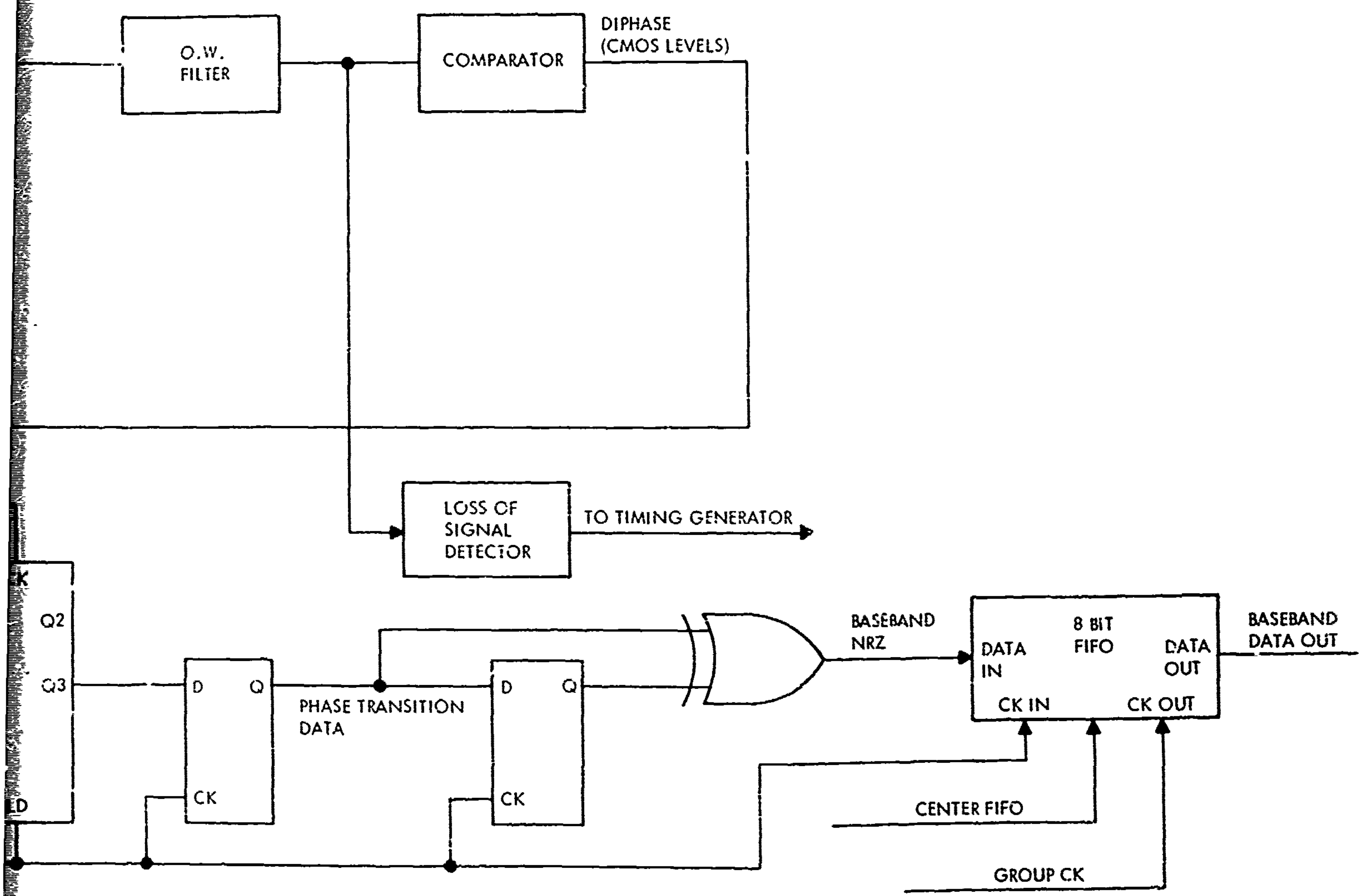
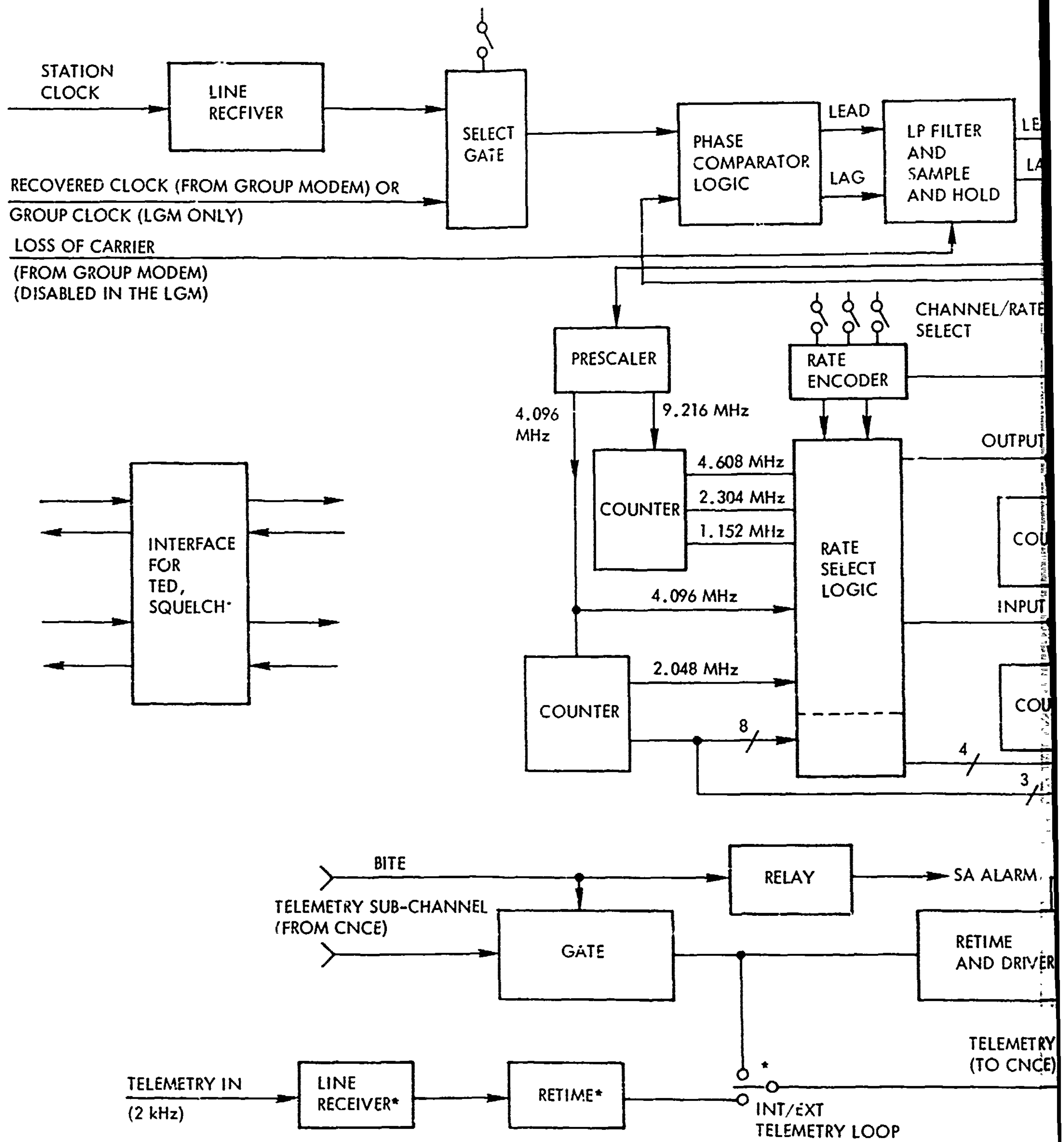


Figure 7-16. Group Modem Demodulator

2



STATION CLOCK
LINE RECEIVER
SELECT GATE
PHASE COMPARATOR LOGIC
LEAD
LAG
LP FILTER AND SAMPLE AND HOLD
RECOVERED CLOCK (FROM GROUP MODEM) OR
GROUP CLOCK (LGM ONLY)
LOSS OF CARRIER
(FROM GROUP MODEM)
(DISABLED IN THE LGM)
PRESCALER
CHANNEL/RATE
SELECT
RATE ENCODER
4.096 MHz
9.216 MHz
OUTPUT
COUNTER
4.608 MHz
2.304 MHz
1.152 MHz
RATE SELECT LOGIC
INTERFACE FOR TED, SQUELCH*
4.096 MHz
INPUT
COUNTER
2.048 MHz
8
4
3
BITE
RELAY
SA ALARM
TELEMETRY SUB-CHANNEL (FROM CNCE)
GATE
RETIME AND DRIVER
TELEMETRY (TO CNCE)
TELEMETRY IN (2 kHz)
LINE RECEIVER*
RETIME*
INT/EXT TELEMETRY LOOP

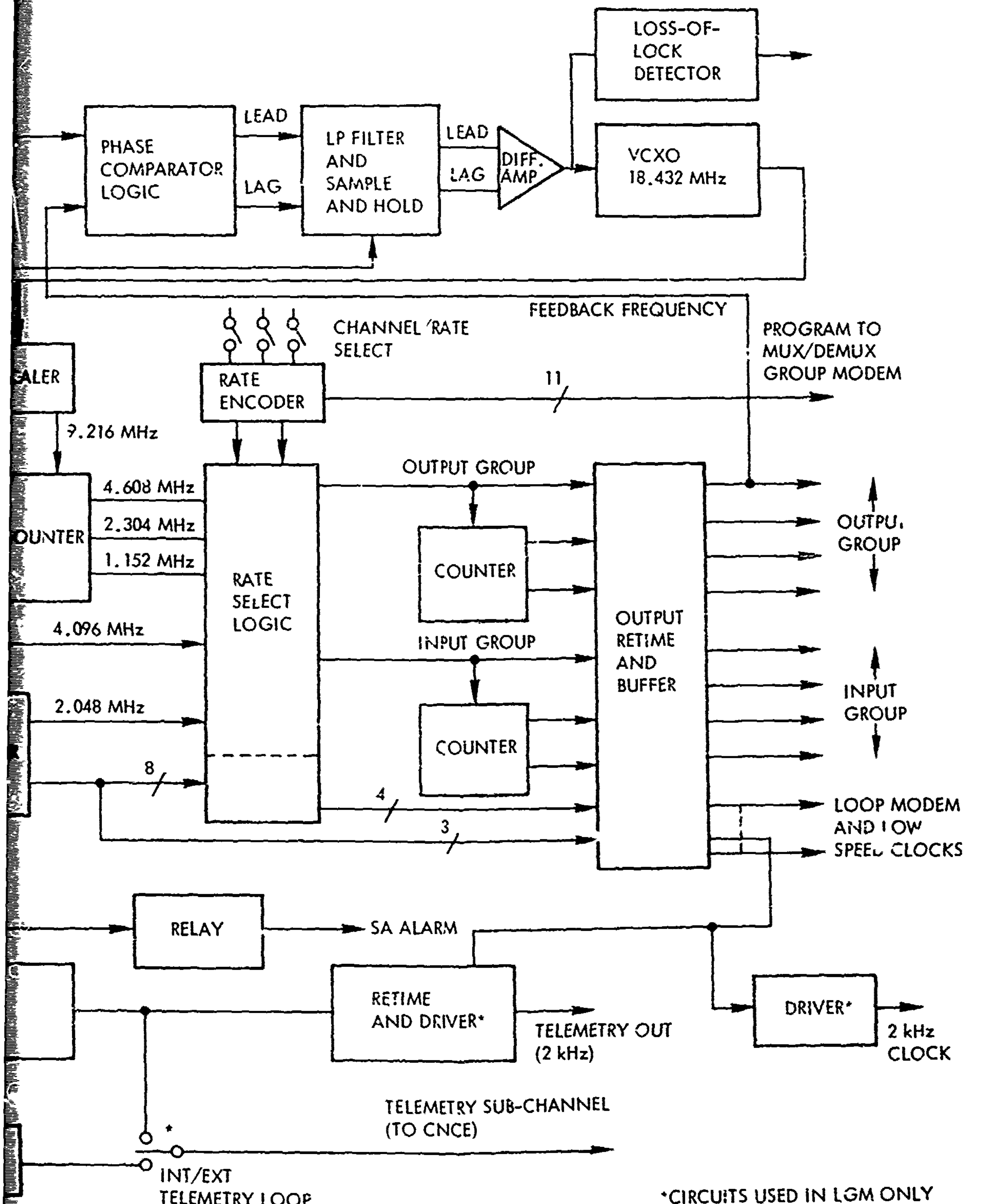


Figure 7-17. RMC Clock and Timing Circuitry

2

TABLE 7-4. TIMING GENERATOR DECODER OUTPUTS

Octal Code	S1	S2	S3	A	B	C	D	E	F	G	H	I	J	K
0	0	0	0	NOT VALID										
1	1	0	0	1	1	0	0	0	0	1	0	0	0	1
2	0	1	0	0	0	0	0	0	1	0	1	1	0	1
3	1	1	0	1	1	0	0	1	1	0	1	1	0	1
4	0	0	1	0	0	0	0	0	1	0	0	0	1	1
5	1	0	1	1	0	1	0	1	1	0	0	0	1	1
6	0	1	1	NOT VALID										
7	1	1	1	1	0	0	1	0	1	0	0	1	1	0
	To Group Modem			To Mux Demux										

SWITCH INPUTS (S1, S2, S3).

A voltage controlled crystal oscillator (VCXO) is used as the prime clock generator. All clock outputs are derived from this oscillator by count-down logic and passed to the output pins by selector gates. The count-down logic is shown in Figure 7-17. In that figure the output of the VCXO is applied to a prescaler circuit which divides by 2 and by 4-1/2 to generate 4.096 MHZ and 9.216 MHZ. Clocks are generated by synchronous division of either 4.096 MHZ or 9.216 MHZ. One of these clocks is selected for further division to create a family of clocks associated with either the input group (low group) or output group (high group). In addition, a group of clocks will be generated to operate the Loop Modem and the Group Framing cards. In addition, a 2 KHZ clock is generated to operate the SYSCON Telemetry access interface and a 150 HZ clock is generated to operate long time-outs on the Group Framing. Included on the Timing Generator are interface circuits for the TED, Frame Squelch, Telemetry data and clock and Station Clock. Gating for the Telemetry is included on the card; when the BITE card declares an SA Alarm, the telemetry subchannel is set to all zeros. In addition, a relay contact is closed to indicate the alarm condition.

The contact closure allows the alarm to be remoted from the unit. In the LGM the SYSCON Telemetry subchannel may be looped around internally or externally by connection of the output to the input through a cable. The mode (internal or external) is controlled by a toggle switch mounted on the front edge of the P.C.B. Since the loop-around feature is internal-only in the RLGM and RMC, the switch is not operative in these units.

The phase-locked-loop portion of the Timing Generator is shown in Figure 7-18. In that figure, the flip-flop is set by a reference feedback clock and reset by the input clock (either the recovered clock or station clock). In the lock condition, the flip-flop output is a 50% duty cycle wavetrain. Each side of the flip flop is intregrated by R_1 and C_1; the resulting levels are applied to a differential amplifier. The output of the differential amplifier controls the VCXO and the loop around the VCXO is closed. When the input diphase is lost on the Group Modem

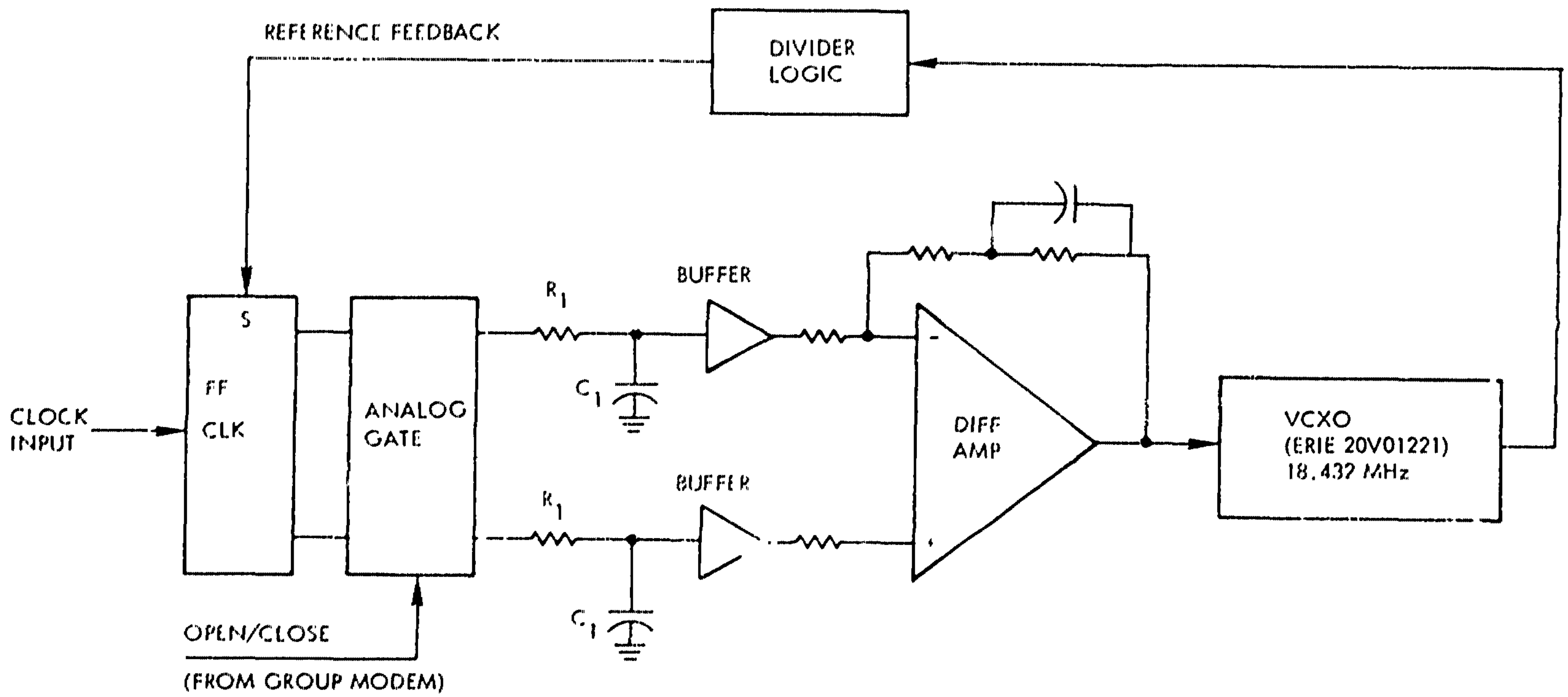


Figure 7-18. Timing Generator Phase-Locked-Loop

the modem generates a control level to open the analog gate. This action holds the last correction value on C_1. The capacitors are buffered by very high input impedance unity gain FET input amplifiers. The control loop is stabilized by the compensation of the differential amplifier. The dominant pole of the PLL is placed at 0.5HZ. The loop shows a slightly underdamped response to input transients. The remaining poles are much higher in frequency and the loop is unconditionally stable with a phase margin of 50° or more at zero gain crossover. The tracking range is nominally $\pm$ 90 ppm when the input frequency is not offset with respect to the VCXO center frequency. The acquisition range is approximately $\pm$ 60 ppm under the same conditions. The range of input frequencies is 576 KHZ to 72 KHZ. The reference feedback is changed as a function of the rate select switches to match the input clock frequency.

Due to the high switching speed involved and the derating of components for temperature, reliability, and nuclear effects, it was necessary to employ Schottky TTL and low power Schottky TTL in addition to CMOS where possible. The majority of the card is low power Schottky logic.

7.3.7 Balanced Interface

A common balanced interface circuit is used throughout the RLGM, RMC and LGM units. Refer to paragraph 3.3.6 for a detail write-up on this interface circuit.

The balanced interface circuits are used on the RMC Station clock input.

7.3.8 BITE

The BITE implementation is similar for all units and is covered in detail in section 5.3.7.

7.3.9 Power Supply

7.3.9.1 Introduction

The Power Supply design represented a most significant technical challenge. The power supplies must have efficiencies of as high as 65% while at the same time be constrained within tightly controlled space and weight restrictions. For this reason, an extensive make/buy evaluation was undertaken. In this regard, there was generated a detailed power supply specification SM-A-876875 and Statement of Work. This power supply specification was submitted to ECOM.

7.3.9.2 RMC Power Supply Design

7.3.9.2.1 Major Performance Requirements

The voltage and current requirements between the RLGM, RMC and LGM units are very closely related. There is, therefore, a common requirement for both the shelter and field units. This similarity resulted in a high degree of Power Supply commonality which has resulted in the utilization of common P.C.B.'s in each of the three units. A total of six P.C.B.'s is required for these units. Table 3-11 shows the utilization, type, and electrical requirements of these modules.

Other performance requirements of the Power Supply are summarized in Table 3-12. These requirements are detailed in the Power Supply specification SM-A-876875.

7.3.9.2.2 Functional Description

A flyback type of converter is used for the DGM power supplies. This type of converter has been used quite extensively in space applications where high reliability and efficiency is a must. A brief description of the basic flyback operation and schematic is given in paragraph 3.3.8.3.2.

The RMC power supply is comprised of modular blocks utilized extensively in the DGM family. A block diagram of the RMC power is shown in Figure 7-19.

Prime power after being pre-conditioned by EMI filters and EMP arrestors is routed to the appropriate AC or DC input network via a relay controlled by a DC sensing circuit. The circuit is configured for AC operation in the non-energized mode; a long time constant prevents dropout, pre-charges the input DC/DC converter filter network to avert current surges through the relay, and prevents inadvertant DC polarity reversal. Figure 3-28 is a schematic of this circuit. A two pole circuit breaker is used on the input. The circuit breaker will break both sides of the line, but will sense only the hot side of the line. Trip points will be set at 3 amps RMS for the 115 V AC operation, and at 15 amps DC for the 28 V operation. Figure 3-29 shows the circuit breaker configuration.

Either a 28 VDC prime input is converted or AC is rectified into a nominal 160 VDC. This high voltage is applied as source power to the flyback converters of the "B" and "D" modules which provide regulation and input/output isolation.

The "B" module converter transforms the high voltage (160 V) DC into pre-regulated DC outputs for subsequent utilization as load supplies, internal bias supplies, or regulation loop control. The "D" converter, converts the 160 V input to a regulated +55 VDC for transmission as source power to the DSVT's and to +180 VDC for remotely powering an RLGM. Various operating conditions such as over and under voltage are monitored.

The RMC internal load supplies are further conditioned by filters and monitored for out-of-tolerance performance and subsequent indication. Separate series regulators are not required since the DC internal load within the RMC is.

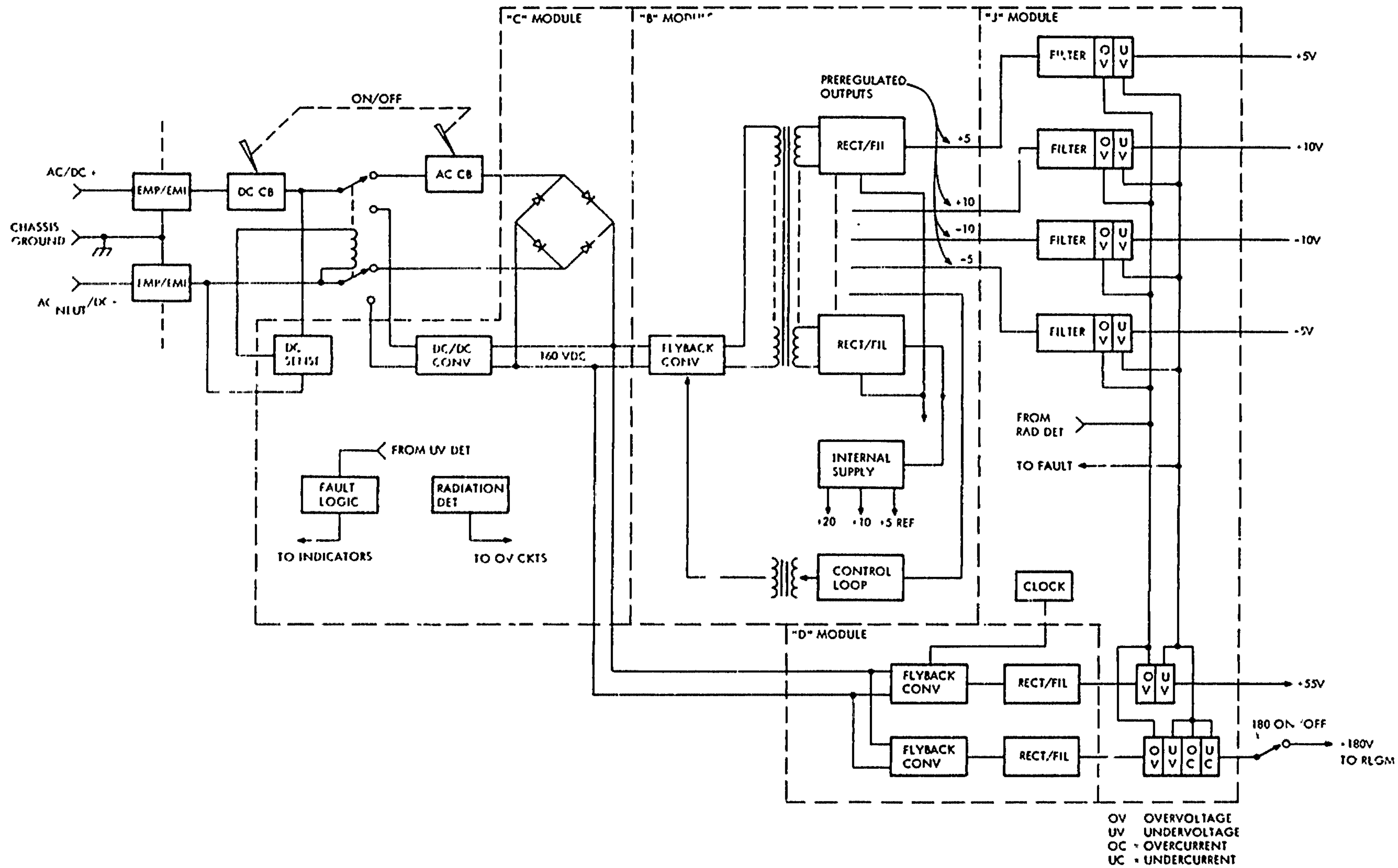


Figure 7-19. RMC Power Supply Block Diagram

low. Consequently, the logic load current variation is minimal. The transformer/regulation loop is sufficiently "stiff" to maintain the ± 5 VDC and ± 10 VDC outputs within the specified regulation range.

Each output status is reported via the undervoltage (UV) summary combiner of the fault logic circuit. An overvoltage (OV) condition is crowbarred to protect the utilizing load and consequently appears as a UV anamoly following cessation of the OV indicated output. Impringing radiation is detected by a radiation circuit which initiates all crowbars, internal and external, to safeguard the load and the power supply.

7.3.9.3.3 PC Card Complement

The power supply modules which are used in the LGM are as follows:

Module Type	Function
J	Consists of the ± 5 VDC and the ± 10 VDC limited range supplies, overvoltage circuits, undervoltage circuits, a clock, power down circuit and some components for the +55 and +180 VDC circuits.
B	Consists of the internal supply and pre-regulators for the series pass supplies.
C	Consists of the DC/DC converter, the radiation detector, and fault logic components.
D	Consists of the +180 VDC and +55 VDC circuitry.

7.3.9.3.4 Technical PC Board Description

7.3.9.3.4.1 Module "C"

This card, shown schematically in Figure 3-30. contains the AC bridge rectifier, the DC DC converter, the fault logic, and the radiation detector. The DC, DC converter is relatively straightforward, although it incorporates a feedback drive with clocked turn-off to facilitate efficiency in drive power and to minimize filter size by guaranteeing a fixed chopping frequency. An interlock assures simultaneous conduction does not occur.

The radiation detector is enabled when the 2N2222 conducts under nuclear bombardment, triggering the monostable. The fault logic combines the UV and test inputs to control the fault relay, fault lamp and power tolerance lamp.

7.3.9.3.4.2 Module "B"

The schematic in Figure 3-31 depicts the flyback converter with its associated control loop and the resultant regulated outputs. This converter employs proportional base drive for efficiency and clocked cycle drive for frequency stability. Source overvoltage protection inhibits operation under input voltage duress and a startup circuit provides reliable initiation. The basic tenent is that energy stored in the primary inductance of the transformer during conduction of the power transistor is transferred to the secondaries when conduction ceases in response to either the regulation loop on a high current sensor. Thus, the circuit is energy limited and behaves, in principle, like the "electric ram".

The secondary outputs are rectified and filtered; some supply the loads, one is used for control feedback, and one generates the +20 V, +10 V, and +5 V reference utilized for internal bias and control.

7.3.9.3.4.3 Module "J"

Refer to Figure 5-16 for the schematic for the "J" Module. The module contains additional filtering for the pre-regulated outputs from the "B" Module. The output of this module is the ± 5 and ± 10 VDC. Overvoltage and undervoltage protection is provided for each voltage output. In addition, a power down circuit is provided for powering down the supply in the event of adverse bias or during radiation conditions.

7.3.9.3.4.4 Module "D"

Module "D", refer to Figure 7-20, is a flyback converter for generating the +55 VDC and the +180 VDC. The +55 VDC is used to power the DSVT's operating in common battery mode. Factory adjustments are provided on this module to set the output voltage and the overvoltage trip point. These are

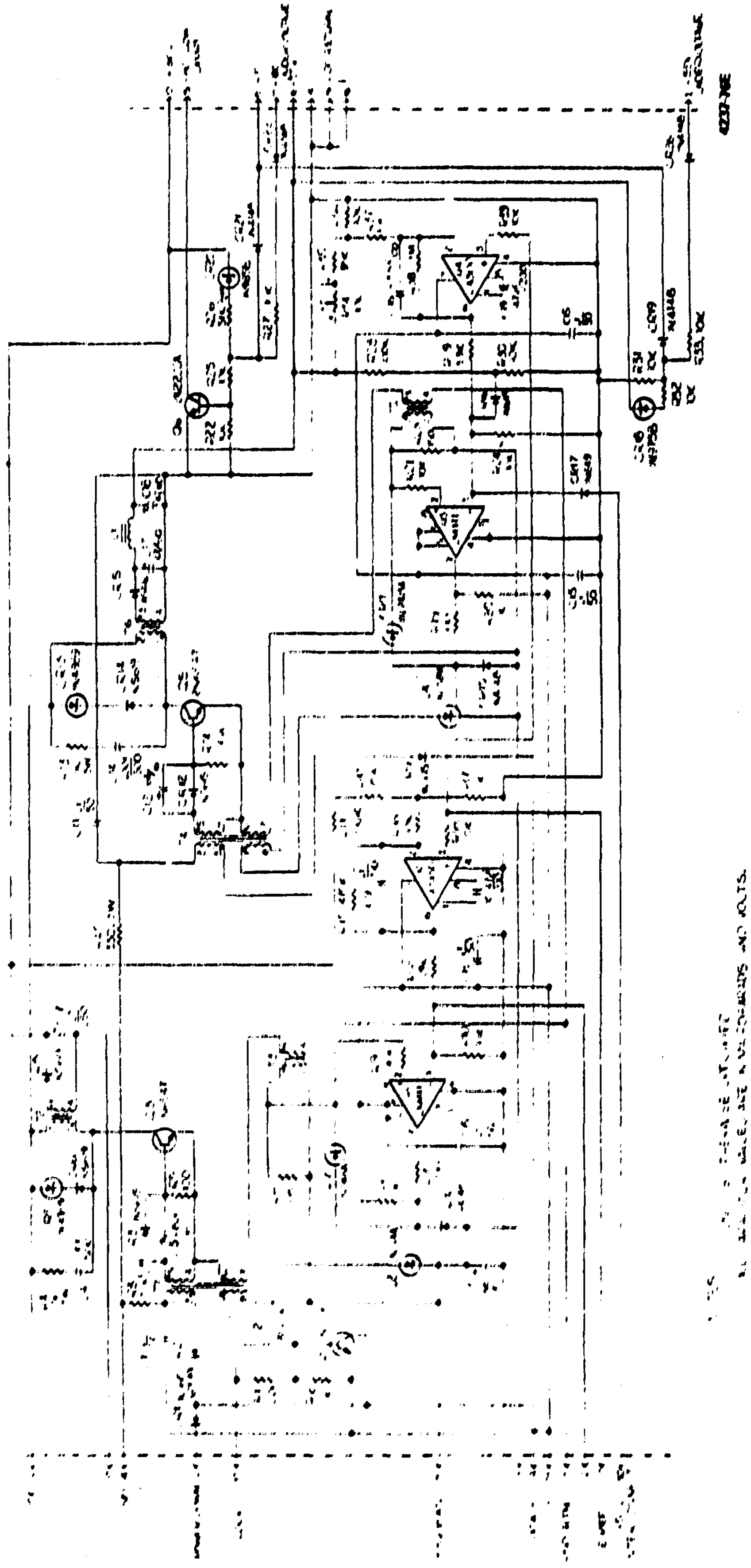


Figure 7-20. Power Supply - Module D

provided because of the extreme voltage tolerances required. The +180 VDC output is used to remotely power the RLGM. A separate +180 Volt ON/OFF switch is provided. The power feed coupling circuits are located within the power supply and are mounted on the chassis.

The operation of the "D" module is identical to the operation for the "B" module. Refer to paragraph 7.3.9.3.4.2.

7.3.10 Signal Entry Panel

The RMC signal entry panel is very similar to the RLGM signal entry panel and differs primarily in the increased number of loop appearences. Details on the protection of circuits terminated on the signal entry panel are discussed in section 5.3.9 of this volume.

7.3.11 Human Factor Engineering

The RMC design incorporates the requirements of MIL-STD-1472B to the maximum extent possible, consistent with operational requirements and physical design limitations imposed by TT-B1-2202-0013 performance specification.

Initial setup controls required to configure the equipment to system requirements are incorporated onto the accessible edge of the PCB's. These controls are protected by the front panel cover. The unit BITE control and alarm are positioned for rapid recognition and ease of identification.

Connections are located on the rear of the case and will be positioned to ensure maximum accessibility.

Unit weights imposed by the specifications are within the requirements of MIL-STD-1472B for lifting and carrying.

Refer to section 15.4 of this volume for detail layouts of the RMC mechanical assembly.

7.3.12 Reliability Design

The RMC has a specified MTBF of 2500 hours. This is equivalent to 400 failures per 10^6 hours.

The reliability prediction and demonstrated results are summarized in Table 7-5.

TABLE 7-5.

RMC RELIABILITY

Specified MTBF (Hrs)	Predicted MTBF (Hrs)	Demonstrated MTBF (Hrs)
2500	4508	6300

7.3.13 Summary of PQT Results

The RMC met or exceeded all major functional and environmental requirements. It is to be emphasized that the RMC has successfully passed all of the above tests, as well as all interoperability tests and the out-of-spec conditions found during testing are all of a minor nature and do not affect interoperability. The out-of-spec characteristics are summarized below:

a. Loop output impedance: too high due to high copper losses in coupling transformer.

b. Group interface output impedance: too high at low frequency due to the presence of a dc blocking capacitor in the output.

c. Group Interface alarm: does not always alarm when cable is disconnected.

d. Orderwire Input/Output Impedance: too high due to high copper losses in coupling transformer.

e. Input Power: one unit was above B1 spec value but below prime spec value.

f. Radiation circumvention: slow fall time on 180 Vdc output on power supply when radiation detector was triggered. There is no prime spec for this value.

In addition to the above problems, which will be discussed in Section 7.3.13.1, the RMC had three problems which were discovered and fixed during the course of the testing. One involved the Group Modem. During high temperature test, the Modem, when tested in the High Group position with orderwire present, created excessive errors. The cause was found and corrected; the changes were installed with jumpers on all PC boards. The master pattern has not yet been changed for the final design. The second problem was a water leak during immersion testing. The cause was found to be excessive weld metal removal around the handle recess in each end of the equipment case causing a small crack to form on that seam. The units were repaired with epoxy applied to the inside of the seam for a water-tight seal. The third problem was a failure during vibration test. The cause was traced to the use of the mounting bracket during these tests. The bracket was redesigned and the retest was successful.

7.3.13.1 Problems/Solutions

The problems encountered during the testing of the RMC were not major and do not affect the mission of the equipment. Some of the problems, such as the Loop Modem output impedance, are common to the RLGM and LGM. Most of the problems are at the interfaces where the RMC inter-operate properly, the interface specifications are not all met. Many specifications are too conservative and represent too pessimistic a view of the interface requirements for proper operation. The problems are presented below.

7.3.13.1.1 Loop Channel Output Impedance

The requirement in electrical characterisitcs testing for loop channel output impedance (Paragraph 12.16, Step 2 of F001) is that the output impedance be 125 ohms $\pm$ 15% at 8, 16, 32 and 56 KHz. This requirement is also in the DGM Family Interface Control Drawing 910669, Paragraph 1.4.1.b.

The impedances measured between 146.2 ohms and 171.3 ohms. The impedance out of tolerance is due to copper losses in the output coupling transformer and can be corrected by changing a series output resistor per loop channel (R38 and R50) from 120 to 91 ohms. This change would bring the impedance in specification.

There is no need to change the loop output impedance at this time as it does not impair the ability to use the DSVT. The multiplexer RMC operates error free for all cases of cable length and frequency with the DSVT.

For this contract, a waiver has been requested (waiver No. 029 - Loop Channel Output Impedance) due to the large quantity of printed circuit boards (413) that would have to be changed and the extensive retesting that would have to be done. The change would be incorporated in a subsequent contract.

7.3.13.1.2 Group Interface Impedance

The requirement for group interface input impedance at the time electrical characteristics tests were performed was 58 ohms ± 15% specified from 300 Hz to 3 MHz. This requirement is paragraph 12.25, Step 4 and 12.29, Step 4 of Electrical Characteristics Tests F001 and Paragraph 1.2.1.e of the DGM Family Interface Control Drawing 910669.

The high group interface has a large capacitor (1.2 μf, 200 Vdc) in series with the terminating resistor to protect the input stage of the group modem if the 180 power feed is accidentally connected to the high group interface measured 300 Hz ranged from 105 ohms to 113 ohms. This data is inaccurate because the measurement technique used did not allow for any reactance impedance due to the capacitor. The actual magnitude of the input impedance is 89 ohms obtained by both calculation and measurement which is, however, still above the specification value of 58 ohms. Because of the physical size of the capacitors (input and output) on the group modem CCA, making it impractical to use larger capacitors, the requirement has been respecified in the DGM Family Interface Control Drawing to 100 maximum 300 Hz to 1 KHz; 58 ohms ± 15% 1 KHz to 3 MHz. The current design does not affect any other specifications or impair the group signal or orderwire performance of the high group interface and meets the impedance requirements as respecified.

For the low group interface, the power feed circuitry located in the power supply is in series with the terminating resistor. This circuitry consists of a series 10 μf capacitor and a 50 mH inductor effecitvely to ground.

The circuitry is used to couple the 180 volt power feed of the RMC onto the cable and also to isolate the power feed from the group modem CCA. The input impedance of the low group interface of the 4 RMC's tested ranged from 70.9 ohms to 77 ohms measured at 300 Hz. Unlike the high group, this data is within 3% of the actual value because the phase angle of the impedance obtained by both measurement and calculation is less than 10^{o}. The current design does not affect any other specifications or impair the group signal or orderwire performance and meets the impedance requirements as respecified above.

7.3.13.1.3 Group Interface Alarm Signal

Paragraph 1.2.1.F of the DGM Family Interface Control Drawing 210669 requires that the group interface have an alarm threshold on the incoming received signal. This requirement was measured as part of Electrical Characteristics Tests F001 Para. 12.25, Step 72 for the high group and Para. 12.29, Step 72 for the low group. The RMC does not meet this requirement in that an alarm is not always indicated when the input cable is disconnected. This is a result of the reference side of a comparitor being set too low and the comparitor being triggered on noise. A change in resistor (R40) from 12 ohms to 36 ohms would raise the reference voltage and the alarm detector would work properly. This resistor is located on the group modem CCA.

For this contract, a waiver has been requested to allow the use of the group modems as there is no need to change the resistor at this time. The operation of the modem is not affected by the alarm detector working improperly. The alarm is used only for BITE and would not give a false alarm but only a lack of alarm when the input cable is disconnected. To incorporate the change would require shipment, document changes, changing the resistor, rework of conformal coating and testing of the 57 printed circuit cards. The resistor would be changed or a new alarm circuit designed with greater noise immunity at high frequencies for a future production contract.

7.3.13.1.4 Orderwire Input/Output Impedance

Para. 12.26, Step 5 and 10 and 12.30, Steps 5 and 10 of Electrical Characteristics Tests F001, para. 1.7.B of the DGM Family Interface Control Drawing 910669 and Para. 3.1.2.4.2 to the RMC Prime Item Development Specification 11300C require that the orderwire input/output impedances be 600 ohms ± 10%.

The input and output impedances ranged from 682 ohms to 721 ohms. The failure is caused by failure to make allowance for the copper losses in the orderwire transformers at the time of the design. What is needed to bring the impedances within the limits of the specification is to change two series resistors, one for the output impedance and one for the input (R13 and R19), from 560 ohms to 470 ohms on the Group Modem CCA.

For this contract a waiver has been requested (waiver No. 032 Orderwire Input/Output Impedance) to allow the use of the RMC as is because the ability to use the COU is not affected. The current design meets the requirements of orderwire insertion loss Para. 1.7, Table IV of 910669 when interfaced with all the applicable equipments of the DGM family. Changing the impedance on both ends of an orderwire link over two miles of cable would only improve the insertion loss by 1.5 dB out of 40 dB. To incorporate the change would require shipment, document changes, changing the resistors, rework of conformal coating and testing of the 57 printed circuit cards. The resistors could be changed on a production contract.

7.3.13.1.5 Input Power Test

Para 12.14, Step 42 of Electrical Characteristics Tests F001 requires for all conditions of input voltage with the range of 115 Vac ± 10%, 50 to 400 Hz ± 5% or 28 ($^{+4}_{-6}$) Vdc the input power shall be no more than 190 watts. This requirement is also Para. 3.1.2.7 of the RMC Prime Item Development Specification 11300C.

The RMC requires the greatest amount of input power when operating on 22 Vdc and for this condition one of the four (4) RMC's tested, serial number 14 failed the specification, requiring 191 watts.

This input power, however, is for a full load on the power supply which would not exist in any of the configurations of the RMC. The RMC cannot be configured to use an RLGM on the low group and provide power feed to the RLGM and at the same time provide power feed and signal to 8 loop interfaces. The most loops that can be used when interfacing with an RLGM on the low group is four (4). Powering four (4) loops rather than eight (8) reduces the power load by approximately 14 watts. If eight (8) loops are to be powered, the RMC cannot interface with an RLGM on the low group; therefore, the input power to the RMC would be reduced by approximately 75 watts.

Because RMC power supply is to be tested and specified under full load, the requirement for maximum power has been changed to 210 watts.

7.3.13.1.6 Radiation Circumvention - 180 Volt

Para. 12.14, Step 42 of Electrical Characteristics Tests F001 and Para. 3.2.1.12.3 of the RMC Prime Item Development Specification 11300C require that power supply outputs circumvent upon exposure to a dose of gamma radiation to protect the internal circuitry of the RMC.

For the 180 volt output, the requirement at the time electrical characteristics test were performed was that the output had to be reduced to less than 100 V - 100 s after initiation of the test pulse into the radiation sensor and less than 30 V - 400 μs after initiation of the pulse.

Because the 180 volt output of the power supply does not supply power to any circuitry within the RMC, it is not necessary to reduce the 180 volt output to insure the survivability of the unit. The requirement for 180 volt circumvention has, therefore, been removed from the RMC specifications.

15.4 MECHANICAL DESIGN - LGM, RMC AND RLGM

15.4.1 Shelter Mounted Unit (LGM)

15.4.1.1 Case Design

The LGM shelter mounted unit (see Figure 15-1) is packaged in dip-brazed equipment case 8-1/2" high by 12" deep by 17.25" wide, fabricated from 6,000 series aluminum alloy plate and extrusions. Dip-brazing yields the most practical and versatile method to obtain good working tolerances and a good production yield for equipment case/chassis of this type, while providing cost effective joint design for suppression and control of EMI and RFI.

The equipment case is designed to accept mounting brackets similar to SC-B-627147; the four bracket mounting holes are located 3-3/16 inches back from the front edge of the case on both sides. Two carrying handles are mounted to the equipment case forward of the mounting brackets and positioned so as not to interfere with the ability to rack-mount the equipment in a standard electronic rack having dimensions conforming to MIL-STD-189.

Captivated, 10-32 thread, blind inserts are provided in the wall of the case for the rack-mounting brackets.

The shelter mounted LGM equipment case is an integral assembly conforming to MIL-T-4734, constructed of aluminum alloys bonded by dip brazing techniques. Materials, parts and processes are in accordance to MIL-P-11268. The finish is in accordance with MIL-F-14072; the unit is painted with light grey enamel in accordance with TT-E-529, color No. 26250 in accordance with FED-STD-595; front panel marking is Group 1 in accordance with MIL-M-13231.

The equipment case houses two major functions - the power supply and the plug-in PCB assemblies. The case design permits added isolation of these two major functions by installation of a vertical partition if required. The LGM designs obviate this need from a signal or thermal consideration. All plug-in

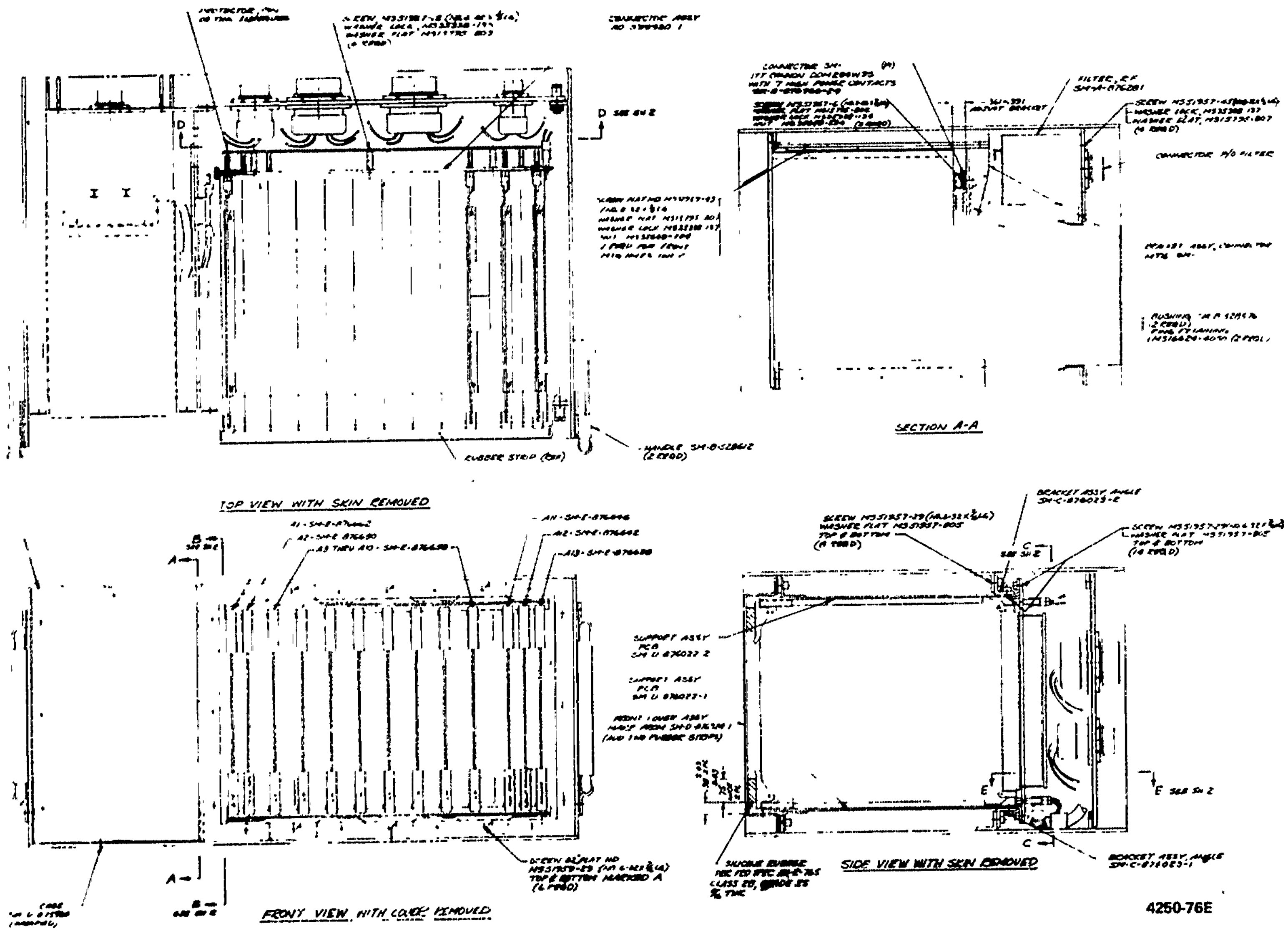


Figure 15-1. Loop Group Modem (LGM)

subassemblies, i.e., power supply and PCBs are replaceable from the front of the unit. A removeable RFI gasketed cover complete with captive hardware encloses the PCB compartment.

All normal operational and hook up connectors are located on the rear surface of the unit. A rear cover provides major maintenance and initial installation access to the wiring of the wirewrap panel. All operational controls are front panel mounted at the power supply immediately accessible to the operator. Localized fault locating is provided on each plug-in subassembly.

15.4.1.2 Printed Circuit Card Design

The DGM shelter mounted and Remote equipments with the exception of the Cable Orderwire Unit (COU) and the Pulse Restorer (PRS) uses a standard sized plug-in PCB. The standard panel features a 112 pin male blade connector and two panel extractors (see Figure 15-2). The layers consist of multiple signal layers with inner voltage layer and a ground layer. LGM PCB's are not dependent on conduction cooling, resulting in a less sophisticated system. Each PCB features positive mechanical keying to prevent incorrect slot insertion. A master keying chart controls interchangeability of PCB's.

An alpha-numeric matrix for the location of DIPs which predetermines the location of the DIP to a grid pattern allows adequate space between DIPs for interconnections and discrete components such as diodes, resistors and capacitors while maintaining established locations compatible with automatic insertion equipment, as needed. The standard PCB excluding the connector and extractor has a component and signal area of 43 inches square. The PCBs are designed to meet MIL-STD-275C, and MIL-P-55640 as applicable.

15.4.1.3 Weight

The basic shelter mounted equipment case less the electronics weighs approximately 4 kg.

The weight of the PCBs average 0.3 kg.

Weight breakdowns and total weights for the LGM are given in Table 15-1.

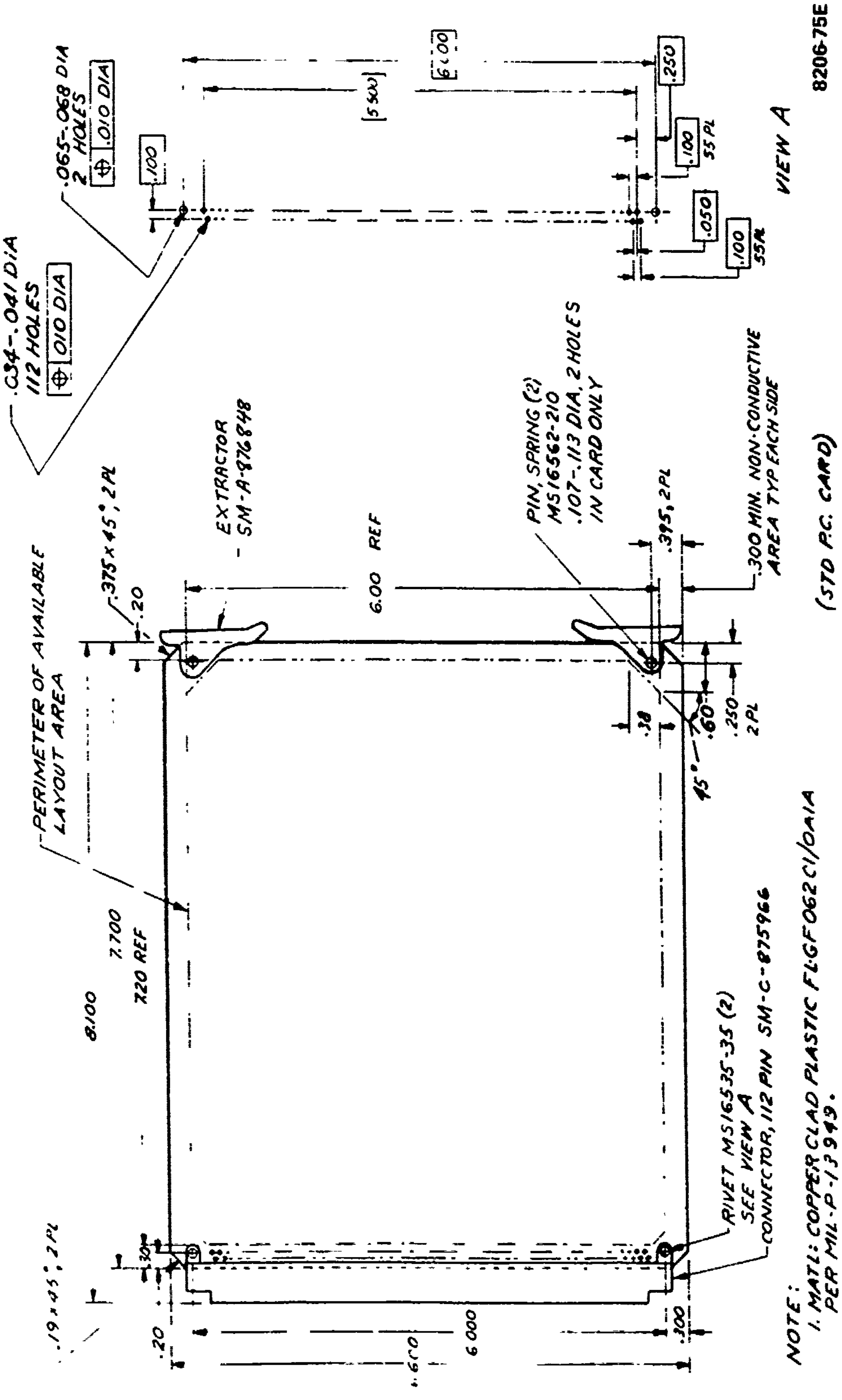


Figure 15-2. Standard Panel

The weight control effort was fully active. As with any formal weight control activity, the initial action was to establish bogies or budgets designed to achieve specification conformance.

TABLE 15-1. LGM WEIGHTS

WEIGHT, KG						
Unit	Case Assembly	PCBs	P.S.	Connector/ Wiring	Total Weight	Specification
LGM	6.6	3.9	3.6	2.0	16.9	17.0

15.4.1.4 Thermal Design

15.4.1.4.1 General

Thermal analysis of the unit and its modules were used as one of the criteria for part selection. Individual modules and units were breadboarded and temperature tested to insure that the design and parts were compatible with the temperatures resulting from the maximum and minimum thermal extremes for the equipment. During the DGM Proposal Phase, preliminary thermal analysis results were used to establish the basic design for the equipments and to select parts 'subassemblies. The LGM closely resembles the physical size, shape, partitioning and fabrication methods of the TD-1065.

Design techniqes used were:

- Use of MIL-Grade, selected components, i.e., 125°C ICs; materials to withstand solar radiation effects and high-low temperature degradations.
- Closed loop convection cooling with direct-to-ambient conduction and convection cooling for P.S.
- Metals and plastics selected for specific proven qualification at extreme low twmperature.
- Use of silicone rubber seals and gaskets rated not to set at levels as low as -70°F.

15.4.1.4.2 Analysis

The preliminary thermal analyses were up-dated for the DGM Shelter type units in an effort to establish:

a. Thermal guidelines for use in the many tradeoff studies which were in progress.

b. Thermal guidelines for use by the mechanical designer in selecting the configuration and the key parts (e.g., card guides) of the subject unit.

c. Thermal guidelines for use by the system engineer/circuit designer in "partitioning" the units.

The following thermal summary provides the final status of thermal dissipations and temperatures on the LGM.

Thermal Summary

There were two major changes in the design path to diminish power dissipations within the LGM.

1. CMOS components greatly reduce power dissipations in the card nests.
2. Custom designed power supplies with 66% efficiencies (with input power at 28 Volts) which enhanced reduced power supply dissipations.

Power Status: Card nest and power supply dissipations are summarized in Table 15-2. This data is compiled based on design goals of a 66% efficient power supply. The highest dissipating card is the timing generator at 5.9 watts.

TABLE 15-2. POWER DISSIPATION

Description	Power
Watts Out	67
Watts in Nest	16.5
P.S. Dissipation	42
*Total	125

*Total power input to power supply (66% efficient power supply)

Environment: The environment to which the units are to be exposed is 145°F.

Relevant Design Details: The LGM is totally closed with heat sinking in the rear of the power supply. Heat sinking will be adequate to dissipate at least 50% of the power supply total dissipation.

The card racks are designed in all cases as to provide at least 0.4 inch between PC cards and case skin to promote convection currents around the cards.

Synopsis: Dissipations were broken down into three sections for analysis.

1. Equipment unit skin to ambient dissipation: In the shelter units, there will be radiation from the rear of the unit to the shelter walls plus free convection from the rear and sides. Also, there will be conduction into the flanges which will mount the units to the rack.
2. Power supply and internal ambient to unit skin dissipation. Convection and radiation will be relied upon for this phase of heat dissipation.
3. PCB, to internal ambient convection dissipation. Conduction, though not relied on for heat dissipation, will render the above summary as conservative.

Results of the thermal analysis are shown on Table 15-3.

TABLE 15-3. WORST CASE THERMAL ANALYSIS RESULTS

	LGM
Case Skin Temp	80°C
PS Case Temp	84°C
PS Transistor Jct Temp	127°C
Max. Allowable PS Transistor Jct Temp	200°C
Average Temp in Card Nest Area	91°C
Max. Internal Ambient Temp in Card Nest Area	99°C
Max. Allowable Internal Ambient Temp in Card Nest Area	135°C
Max. Card Component Case Temp	110°C
Max. Card Component Junction Temp	114°C
Max. Allowable Card Component Junction Temp	150°C

15.4.1.5 Shock and Vibration

15.4.1.5.1 General

Two major areas of concern when considering the design of the equipment to survive vibration and shock include dynamic stresses in the structure, and response of the structures and enclosed elements. Dynamic stresses represent potential problems since material fatigues at stresses well below the yield strength of the mechanical/electrical part or wire connection. Also, excessive deflections between mating or adjacent parts due to resonant response can cause interference and/or subsequent damage.

The LGM utilizes Raytheon's case design which reflects considerable experience over the years with this type of equipment. Also used are developed guidelines and standards to achieve a lightweight vibration and shock-resistant design. The LGM, therefore, enhances product standardization. The guidelines used and a brief discussion of each are presented below:

a. Natural frequencies of major structural items to be as high as practical with 60 Hz being the minimum. It is virtually impossible to design manportable/transportable equipment of this type with no resonances within the range of service frequencies (5 to 200 Hz). Within the constraints of size and weight, the frequency should be as high as possible with the major structural elements having natural frequencies greater than 60 Hz.

b. Resonance conditions are to be analyzed and the stress levels maintained at safe working levels. Static limit load factors will be applied to static structural analysis so that the resulting stresses do not exceed the yield strength of the material and, thereby, ensure that the equipment will function in the dynamic environment. The limit load factors were determined from the vibration and shock requirements of MIL-STD-810 and from an estimate of damping in the structure.

c. Printed circuit board natural frequencies must be at least 1.4 times greater or less than the predominate chassis natural frequency. Parts are located on the board so as to minimize the effects of the part weight (i.e., heavy parts near edges and corners). Relatively large parts (filters, equalizers, etc.) are mounted to the board with threaded fasteners. Relatively small parts (resistors, capacitors, etc.) which weigh more than 1/2 ounce are "strapped" to the board so as not to depend upon their leads for support.

Protective features such as bumpers or mechanical extensions were used to preclude the damage to any part during servicing, handling, or shock. Individual subassemblies will also feature protective elements and careful placement within the outline of the subassembly such that the delicate components are protected by the structure, "roll over" handles, or by other components which can take rough handling without damage.

Knobs, connectors and hardware are recessed within the structure for protection, any protrusion from the basic case/chassis will be limited to rack mounting angles and hook-up cables. Structures and protective features are designed sufficiently rugged to withstand rough handling and normal servicing conditions.

15.4.1.5.2 Printed Circuit Board Analysis

The PCB complement within the LGM shelter package experience identical stress levels and displacements as the other Raytheon Shelter mounted DGM units. Derivation of PCB natural frequency and shock and vibration displacements are referenced to section 15.1.5.2 of volume 1 (Raytheon).

15.4.1.5.3 Vibration Shock Tests for the LGM

Vibration and Shock Qualification testing of the LGM were tested by Raytheon in accordance with paragraph 4.2.6.2.8 of TT-B1-2202-0013 in the following manner:

a. Fixture Design Analysis and calculations was consistent with acceptable practices within the discipline, which result are in the fixture complying with test criteria identified below.

b. Tool control procedures were applied to all fixtures or jigs in accordance with Raytheon General Policies and Procedure No. 61-4350-142 in conjunction with any specific Government agency requirements.

c. Formalized drawings were required for all fixtures or jigs in accordance with MIL-D-1000.

The following procedure standardizes all fixture designs. Resonance surveys were performed on each new fixture configuration prior to vibration test. Once the requirements of this standard were met, no further fixture resonance

investigations were necessary. A 17,500 force pound electrodynamic shaker system was set aside for these tests.

15.4.1.5.3.1 Fixture Evaluation Procedures

Sine surveys were performed in each of the three orthogonal axes with each fixture system assembled in the test configuration. Survey consisted of: 1g: 5 Hz to 200 Hz, 1 oct/min. Prior to fixture surveys, an accelerometer response survey was performed on all accelerometers scheduled to be utilized for these tests.

a. For this survey, all accelerometers were mounted in one direction on the shaker. One accelerometer controlled the performance of the sine survey noted above. All acceleration responses were taped and plotted.

b. Primary areas of investigation were cross talk of the fixture system and verification of vibration input at the mounting points of unit under test conformed to MIL-STD-810.

c. Fixture evaluations were performed utilizing the actual unit or a mass simulating at least the mass weight distribution and CG of the actual test unit.

d. Required data was obtained by the use of tri-axial clusters of accelerometers at the most remote mounting points of the specimen.

   The orientation of these accelerometers was identical to the orthogonal axis designations for the test specimens.

e. The responses of these accelerometers were examined to ensure that motion in any orthogonal transverse direction (cross talk) produced by the fixture did exceed the vibration input levels. (MIL-STD-180)

Sine Survey Criteria

a. Data acquisition and reduction. The following procedure was also applied to actual test item configurations.

b. Data acquisition and reduction. A minimum of four input and cross axes instrumentation points was used. In addition, capability to provide response data of up to 18 response locations on the package was provided as necessary.

c. Accelerometer noise analysis was per[illegible] immediately prior to the first sine survey. The analysis [illegible]isted of taping outputs of the accelerometers (mounted in their correct location on the package) while the shaker system was complete[illegible]y turned on and ready to run except for the gain which remained in the [illegible]nimum position and the oscillator at 5 cps or less.

d. Accelerometer outputs were simultaneously and continuously taped on magnetic tape utilizing a tape recorder with a frequency response of at least 0 to 2500 cps at the recording speed was used.

e. Data at all locations was plotted directly and continuously from the tape producing plots of amplitude (g pk) versus frequency (Hz).

f. All taped data was stored at least until Qualification Vibration Tests were completed to allow analysis of wave shapes should the need arise.

g. Data Acquisition and Reduction. Data Acquisition and playback system had an accuracy of 10%. (Accelerometer output to final chart presentation.)

15.4.1.5.3.2 Shock Test Fixtures

The shock fixture was capable of applying the specified (MIL-STD-810B) shock in each of six directions along three axes with no ringing that would cause peaks greater than the specified input level at frequencies up to 2 kHz. This was demonstrated by a Polaroid[R] photograph of the input shock pulse at each input location. The instrumentation used to observe the pulse was unfiltered to 2 kHz.

15.4.1.5.3.3 Shock Tests

The shock pulse was also recorded on magnetic tape at each of the input locations and at least two other response locations in the package for a minimum of six instrumentation points. The data will remain on tape for further analysis if it becomes necessary.

15.4.1.5.3.4 Instrumentation - Vibration Tests

The Tri-axial clusters described consisted of commercial tri-axial piezo-electric accelerometers mounted on the appropriate faces of a small mounting cube. This cube was subsequently mounted at the desired location on the test specimen or fixture.

15.4.1.5.3.5 Vibration Tests

The LGM was subjected in all three orthogonal axes in the following tests:

*Test Level - 1.5g (as limited by 1" P-P displacement)
Frequency Range - 5-200-5 Hz log sweep at 1 oct/min
Time Schedule - 5-1/2 hours/axis
Sweep Rate - 5-200-5 Hz in 12 minutes

The unit was functionally tested before and after dynamic tests in accordance with an approved test procedure.

Bench handling shock tests were also performed on the LGM in accordance with MIL-STD-810B, Method 516, Procedure II.

15.4.1.6 EMI Design

15.4.1.6.1 General

The LGM was designed to meet the applicable requirements of MIL-STD-461. A power line filter integral with an external hookup connector was mounted on the rear panel adjacent to an external grounding stud. All access covers, power supply front panel, connectors and external mounted components were gasketed and/or electrically and mechanically bonded to control RFI. Conductive finishes were selected from MIL-F-14072. The LGM was designed and constructed with adequate provisions for bonding the unit to a subsystem ground plane. Bonding is not accomplished through screws connecting the equipment to mounting racks. Bonding jumpers were of the solid metal type and be as short as possible. However, in no case was length to width ratio of the jumper be in excess of 5 to 1. Bonding techniques employed do not impede maintainability nor adversely affect interchangeability. Surfaces being bonded together were prepared by removing all anodic film, grease, paint, lacquer, dirt or other foreign and high resistance materials or agents from the immediate area to insure negligible rf impedance between the adjacent metal parts. Upon completion of the bonding assembly and ascertainment of the

* The level becomes 1.5g at 5.4 Hz or 1.277g at 5 Hz

specified 2.5 milliohm bonding impedance, the completed assembly was refinished in accordance with MIL-F-14072. All panel mounted connectors and components and the panel mating surfaces are free of non-conductive finishes and provide positive bonding and grounding with mating connectors and equipment ground plane. The bonding DC resistance of all connectors and panel mounted components does exceed 2.5 milliohms.

The gasketing systems employed for the LGM did not require rain or immersion seals, therefore, beryllium copper spring finger stock was used. The rear access panel over the W/W plate is E.M.I. protected as is the rear protrusion of the power supply. Captive hardware is located around the periphery of the covers and panels spaced to provide adequate RFI compression without causing unnecessary hardware removal to gain access to the subassemblies for replacement. Shield plates are inserted between subassemblies as required to provide additional isolation of circuits. A summary of the EMI Design is outlined in the following paragraphs.

15.4.1.6.2 EMI Envelope

The outer surface of the LGM was defined as the EMI envelope for design purposes. The unit housing was designed and constructed to provide the required shielding effectiveness. The impedance between any two points on the housing is constant and as low as possible at any frequency. This was accomplished by using highly conductive mating surfaces, close mechanical tolerances, and rigid construction.

15.4.1.6.3 Grounding

The LGM utilizes a multi-point ground, i.e., all signals within the LGM are referenced to a large, easily accessible, low impedance surface area, specifically, the equipment housing. This type of grounding scheme minimizes common impedance sharing between circuits and provides maximum effectiveness from filters, shields, and decoupling networks. Certain high level currents within the system are routed through return wires as required. The LGM is provided with a power safety ground through its I/O connectors. Bonding impedances are less than 10 milliohms measured at dc.

routed through return wires as required. The LGM is provided with a power safety ground through its I/O connectors. Bonding impedances are less than 10 milliohms measured at DC.

15.4.1.6.4 Ventilation

Forced cooling air, internal to the unit, was not used. Closed loop convection internal cooling was employed. Therefore, EMI integrity was not compromised due to cooling requirements.

15.4.1.6.5 Printed Circuit (PC) Boards

PC boards with ground planes and more than three chassis ground connections are far superior to those with grounds which are interspersed among the interconnecting etches. The ground plane minimizes common impedance sharing between circuits on the board and also acts as an RF shield to reduce board-to-board coupling. When multi-layer PC boards are used, a ground plane is a practical necessity, and was used.

15.4.1.6.6 Internal Wiring

In an equipment which processes only digital signals, the internal wiring arrangement is less critical, since practically any configuration will be adequate. However, when an equipment processes digital, analog, and high-level continuous wave (CW) signals, the layout becomes critical because of coupling within the wire harnesses. The two factors which reduce cable coupling are use of shielded cables which are properly terminated, and physical separation. These techniques were used in the design of all the DGM units.

15.4.1.6.7 Switches and Indicators

All external switches utilize grounded shafts. Indicator lights are shielded as necessary.

15.4.1.6.8 Power Supply

Power supply noise and operational signals at the power supply input are reduced to the lowest possible levels through design. This resulted in lower

insertion losses for the power-line filter, which reduced filter size and cost. A solid-grounding approach also helped reduce power supply noise.

15.4.1.6.9 Filter Installation

There are two major criteria involved with filter installation. First, the output wires must be isolated (shielded) from the input wires by at least the insertion loss of the filter. Second, the case of the filter must be referenced to the same ground point as the signals it will attenuate; that is, the RF impedance between the installed filter and the signal reference must be as close to zero as possible. This type of filter installation was used as it achieves maximum insertion loss from the filter.

15.4.1.6.10 Access Panels

Panels, as described, were held to a minimum with least peripheral length to complement EMI seal.

15.4.1.6.11 RF Gaskets

For maximum shielding effectiveness, a gasket must mate with clean and rigid surfaces, must have resiliency, and must be uniformly compressed more than 50%. Therefore, screw spacing for the mating surfaces was selected in accordance with Figure 15-3.

15.4.1.6.12 Required Shielding Effectiveness

Each unit enclosure was designed to provide 80 dB of shielding effectiveness. This provided sufficient attenuation to reduce all radiated signals to levels below the MIL-STD-461A and Tempest limits. A view of the LGM is shown in Figure 15-1. The basic frame is dip brazed construction. The front and back covers are sealed with an RF gasket and bolted into place. All gasket mating surfaces are finished with irridite to prevent corrosion, but this finish does not degrade the shielding effectiveness as the gasket bites into the frame when the covers are secured.

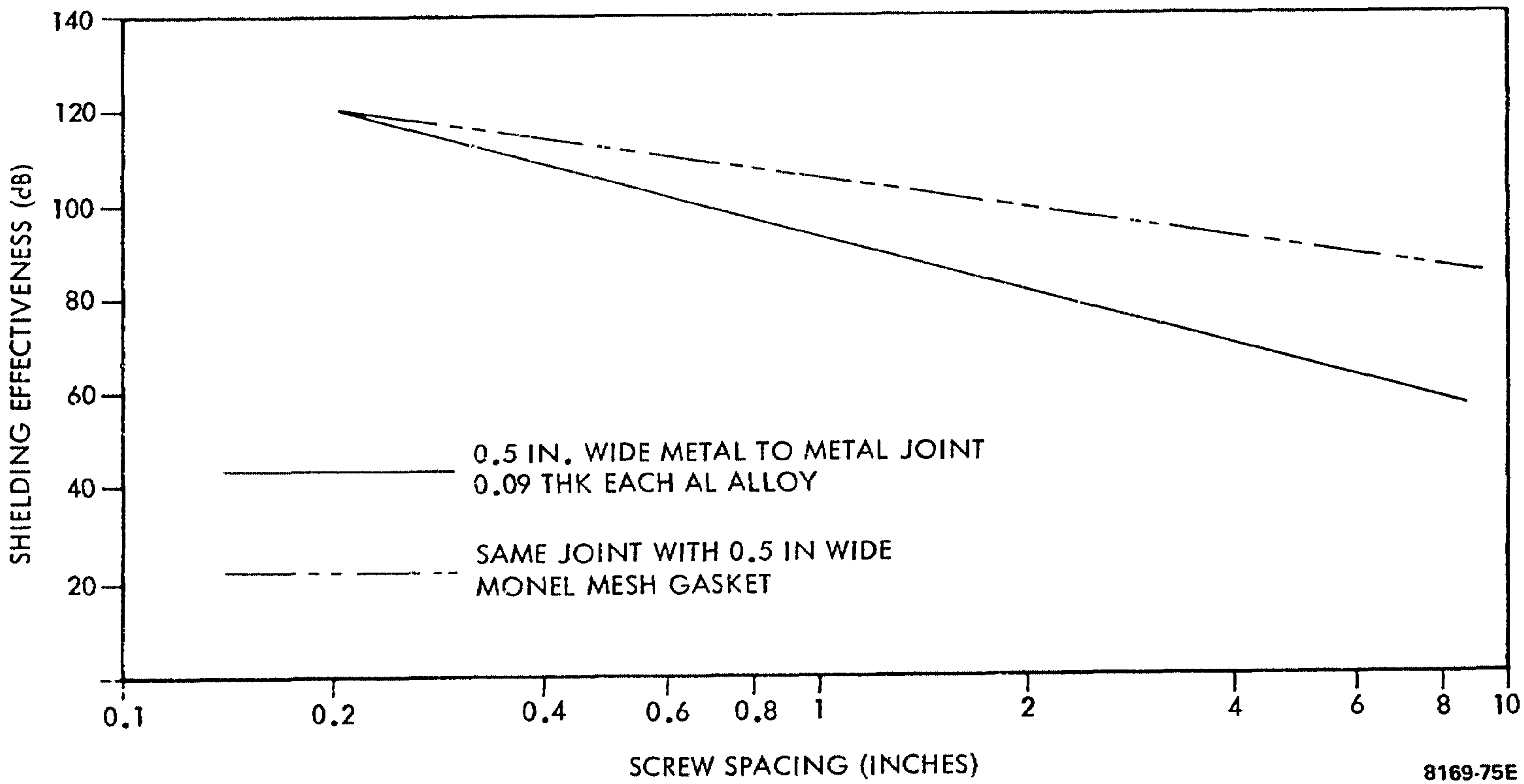


Figure 15-3. Shielding Effectiveness vs. Screw Spacing (Frequency = 200 MHz)

15.4.1.7 Humidity, Salt Atmosphere, Fungus

Humidity and salt atmosphere conditions as invoked and characterized by the MIL-STD-810B tests can result in moisture migration and penetration and a high level of corrosion. To achieve a humidity/corrosion resistant design, the following design criteria were used through all levels of design:

a. Use of non-metallic materials which are non-hygroscopic or have very low water absorption characteristics
b. Observance of the compatible couple requirements of dissimilar metals
c. Use of protective finishes to increase corrosion resistance of metals
d. Corrosion resisting stainless steels for hardware
e. All active semiconductor devices hermetically sealed
f. Use of conformal coatings (per MIL-I-46058) for printed circuits to protect against corrosion and to inhibit short circuiting due to humidity and/or dust
g. Careful attention in the selection of traditionally troublesome components such as potentiometers and coils
h. Careful control of printed circuit board materials and fabrication processes
i. Use of non-nutrient materials in accordance with MIL-STD-454B, Requirement 4, e.g., G10 Series PC Cards
j. Sealed and pressure relieved case design
k. Gasketed covers

15.4.1.8 Power Supply

The power supply was designed as a separable plug-in subassembly mating with rack and panel style connectors at the rear and mounting via captive hardware at the front of the equipment case. The LGM incorporates a finned (heat sink) rear panel on the power supply, protruding through a gasketed opening in the equipment rear panel. Design of the fin assembly requires that 50% of the Power Supply dissipation transfers directly to outside ambient at a minimum. Closed loop convection will be utilized for the balance. Figure 15-4 shows the

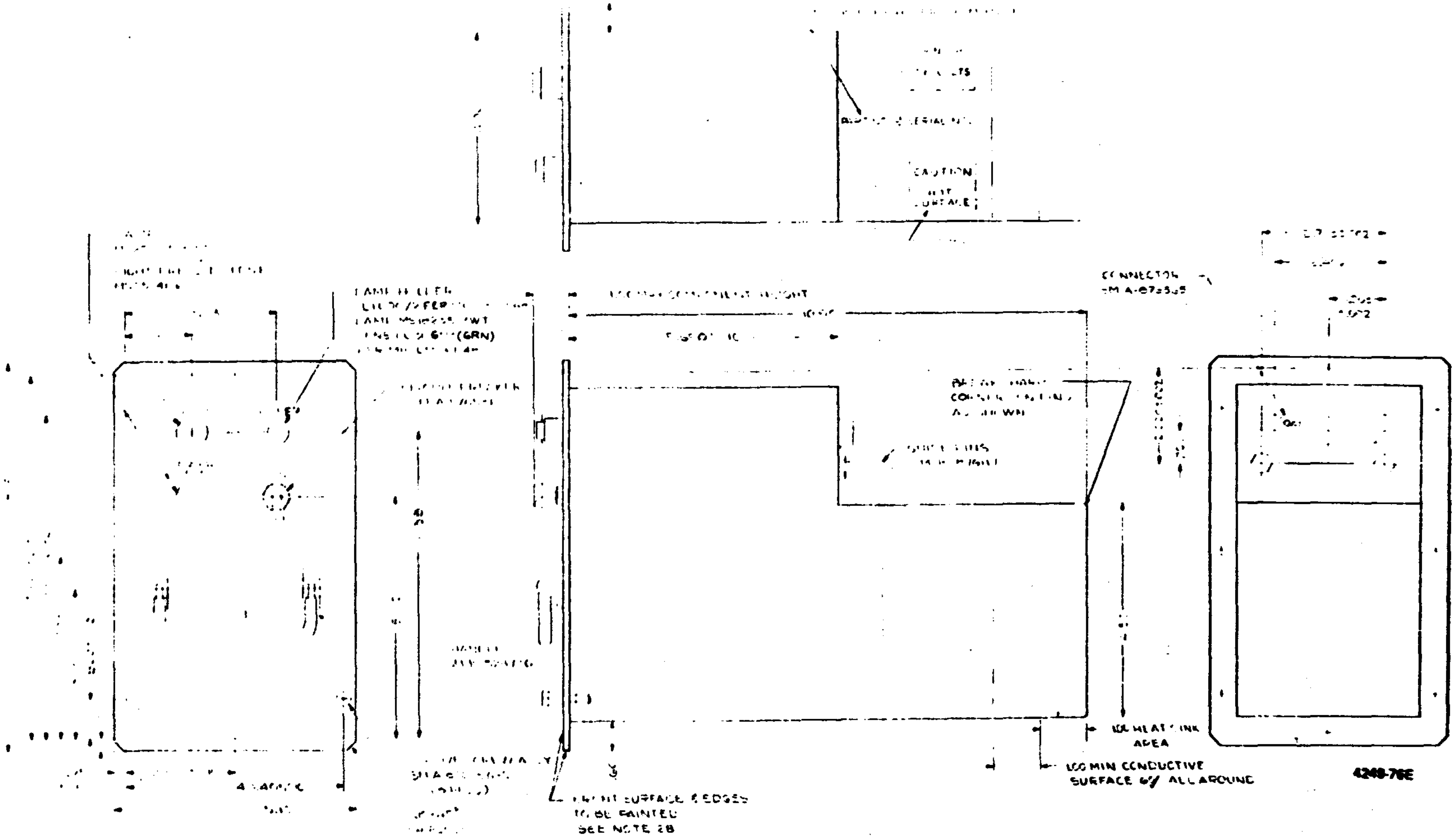


Figure 15-4. Power Supply - LGM

P. S. configuration. However, all supplies including those for the Remote RMC and RLGM use common sub module assemblies. The general construction is accomplished by use of a machined plate type of enclosure.

The Power Supply houses four modules (as listed in Table 15-4). Each module is a plug-in type of P. C. board. The major heat dissipating component is mounted on a metal heat sink which is an integral part of the board assembly. These heat sinks are mounted to the finned heat sink on the unit by hardware which is accessible from the rear of the power supply. The front edge of all boards is secured by a card guide. Both the upper and lower edge of the board are held in place by retaining bars. The front compartment provides clearance for front panel components. Some components are also mounted directly to the case structure.

The overall P. S. unit as noted earlier is serviceable as a subunit from the front of the LGM. A system of guide tracking is provided to allow for direct insertion of the supply into the LGM. Shock blocks and pin engagement provide the mechanical interface at the rear with positive automatic engagement of the rear connectors. As the engagement is accomplished, the supply is lifted by the tapered shock block pins off the unit slide track. The front panel fasteners then accomplish the final mechanical lock.

TABLE 15-4. LGM POWER SUPPLY ASSEMBLIES AND ALLOCATIONS

1.	(A Module)	1
2.	(B Module)	1
3.	(C Module)	1
4.	(H Module)	1

15.4.2 Remote Units

15.4.2.1 Case Design

The RMC and RLGM (See Figures 15-5 and 15-6) are units designed to be operated in an exposed field condition or in shelters and vans. When in an operating mode, the unit is 8.5" high, 13" deep and 17.50" maximum wide and is fabricated from aluminum alloy sheet welded to an extruded framework. Welded interfaces provide the required EMI attenuation. Details of the case are shown on Figure 15-7. Four captivated 10-32 blind inserts are loacted on each side, 3-3/16 inches back from the front edge of the case, where the case width is 17.25 inches. Standard rack mounting brackets similar to SC-B-627147 can be installed in the inserts to adapt the case from a field case to a case compatible with MIL-STD-189 racks.

Two carrying handles are provided on the case in a manner to permit the unit to be readily transported. The handles will be of the spring return type to fold out of the way when the unit is rack mounted.

Materials, parts and processes are in accordance with MIL-P-11268. The finish will be in accordance with MIL-F-14072. The units are olive drab, color No. 24087 of Fed-STD-595.

Within the case are two compartments, a large area on the right for the plug-in printed circuit boards and an area on the left for the plug-in power supply. The PC boards are installed from the front of the unit, sliding on minimum friction plastic card guides until the 112 pin connector on the card mates with its keyed connector on the card nest. Cards are retained in the case by means of a front panel which provides positive retention of the cards. Minimum effort is required to remove the cards. Two card extractors on each card are provided to supply a mechanical advantage to aid in the retraction of the card from the nest connector. Once the card is free of the connector, only a light pull on the card extractor is required to slide the card out of the case on the essentially frictionless card guides.

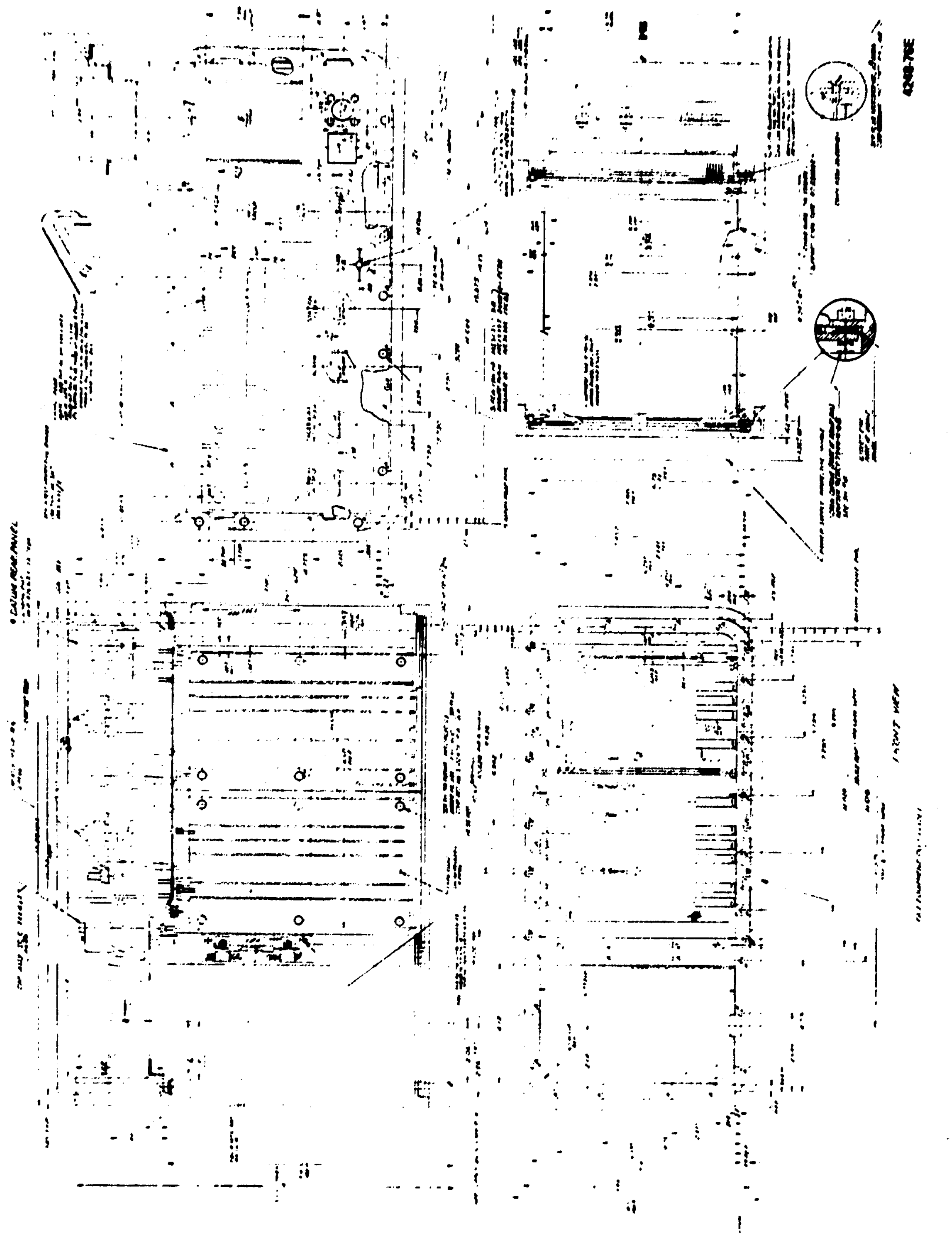


Figure 15-5. Remote Multiplexer Combiner

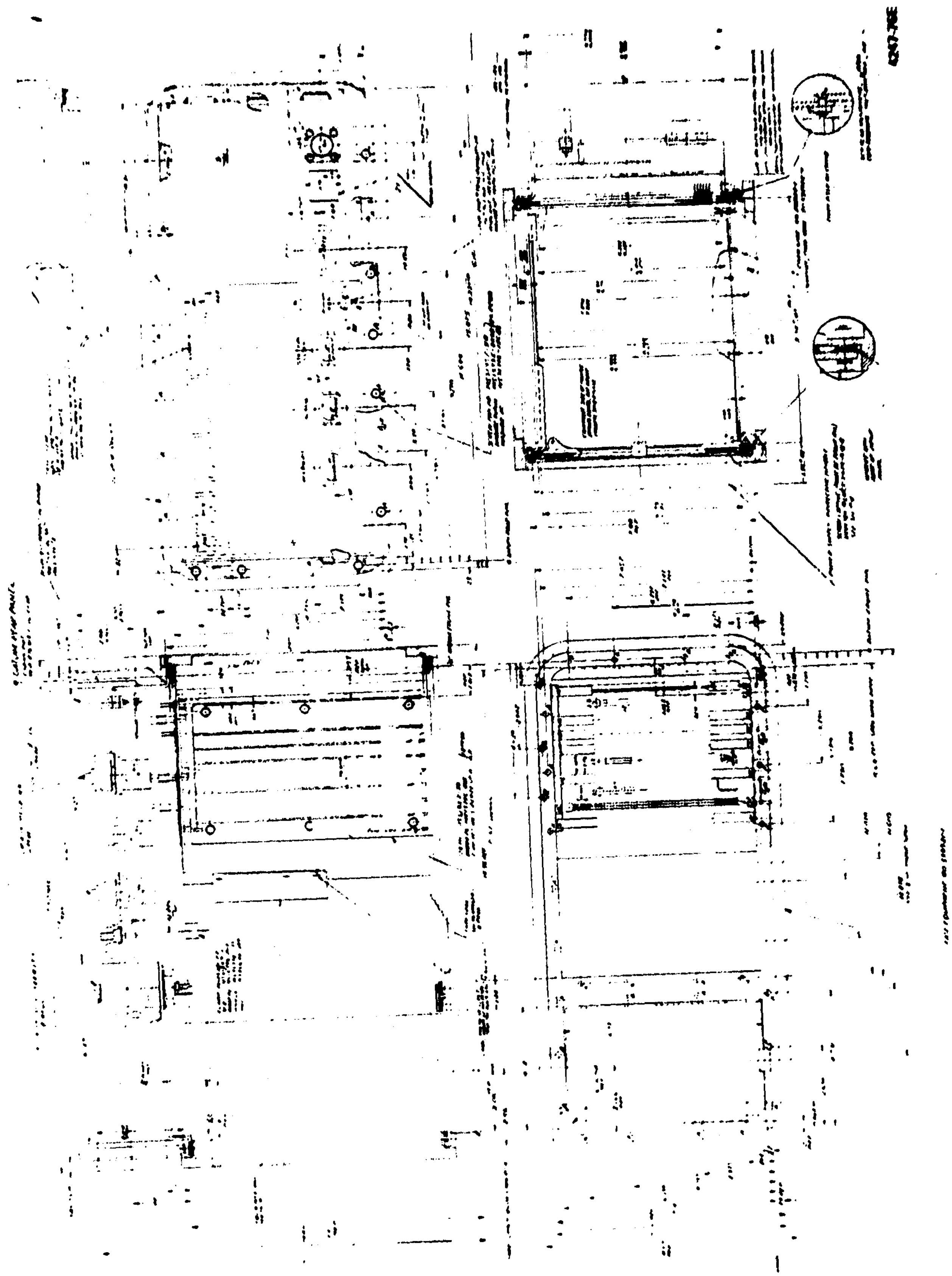


Figure 15-6. Remote Loop Group Multiplexer

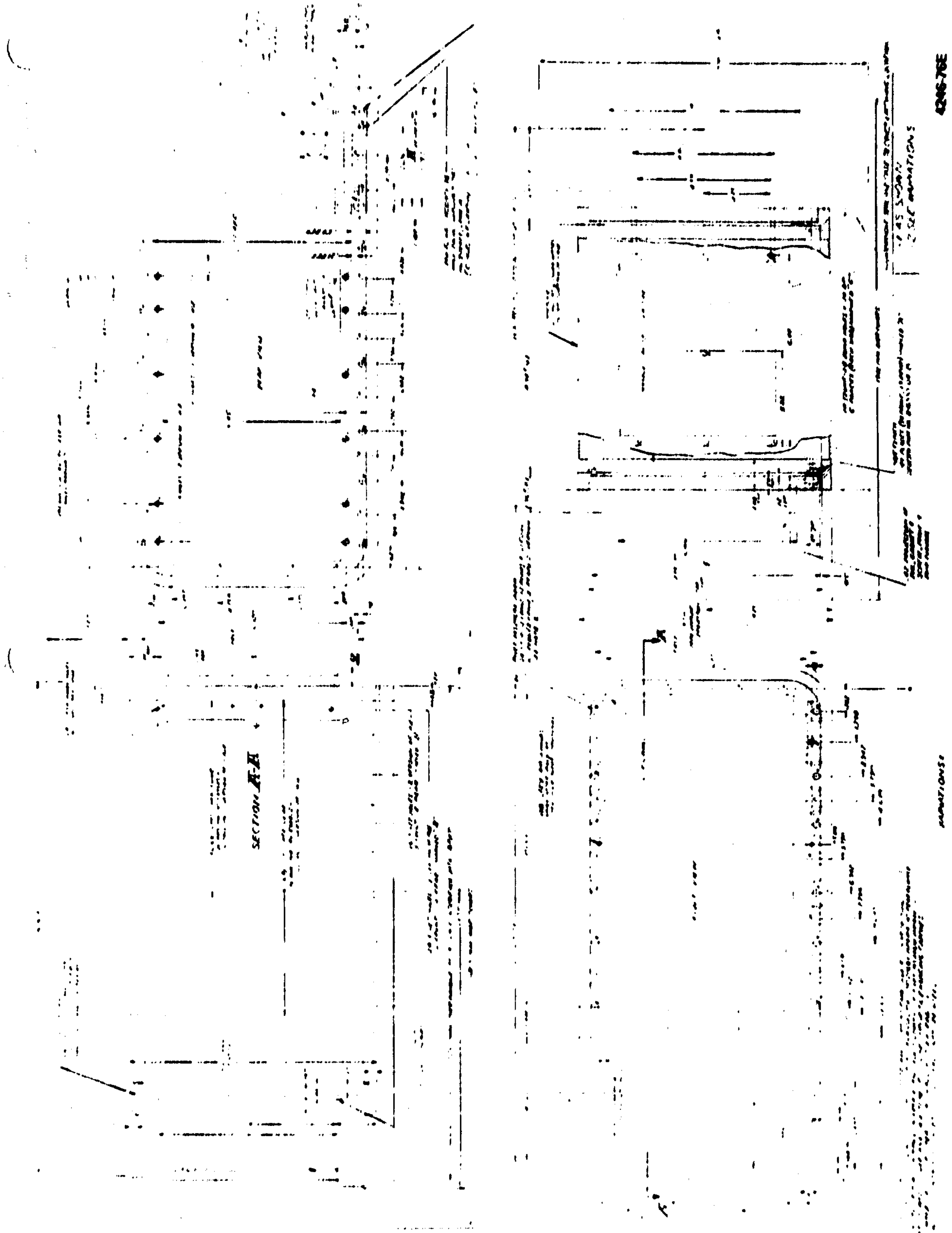


Figure 15-7. Equipment Case

PC access and ease of maintainability has been emphasized. As such, PC insertion and withdrawal factors have been optimized by the following design policies:

a. Clearance type card guides to essentially eliminate that area of friction. Terminal and grounding factors have been designed out of the PC, thus not requiring force contact at the guides.

b. Double purpose ejectors on top and bottom of card height to allow for automatic release from connectors and as hand withdrawal media.

Provisions for guiding the power supply into the case are included. When the power supply is fully inserted, the connectors on the power supply will mate with the case mounted connectors. These interior connectors are mounted such that all power and signal data to and from the power supply are interrupted as soon as the power supply is moved from its normal inserted position. Positive retention of the power supply is provided by screws through the front panel in addition to the shear pins on the rear of the power supply.

All external connectors are located on the rear surface of the unit. A rear cover provides major maintenance and initial installation access to the wiring of the wire wrapped panel.

All power supply controls are mounted on the power supply front panel and are readily accessible whether the unit is being used in the field or in a van.

While being transported, the unit is protected by two covers, one for the front surface and one for the rear surface. The design of the covers is such that the covers protrude beyond each of the basic dimensions of the equipment case to protect the case and all protruding controls, indicators and heat sinks.

15.4.2.2 Printed Circuit Card Design

The DGM shelter mounted and Remote equipments with the exception of the COU and the PRS use a standard sized plug-in PCB. The standard panel features a 112 pin male blade connector and two panel extractors (see Figure 15-8).

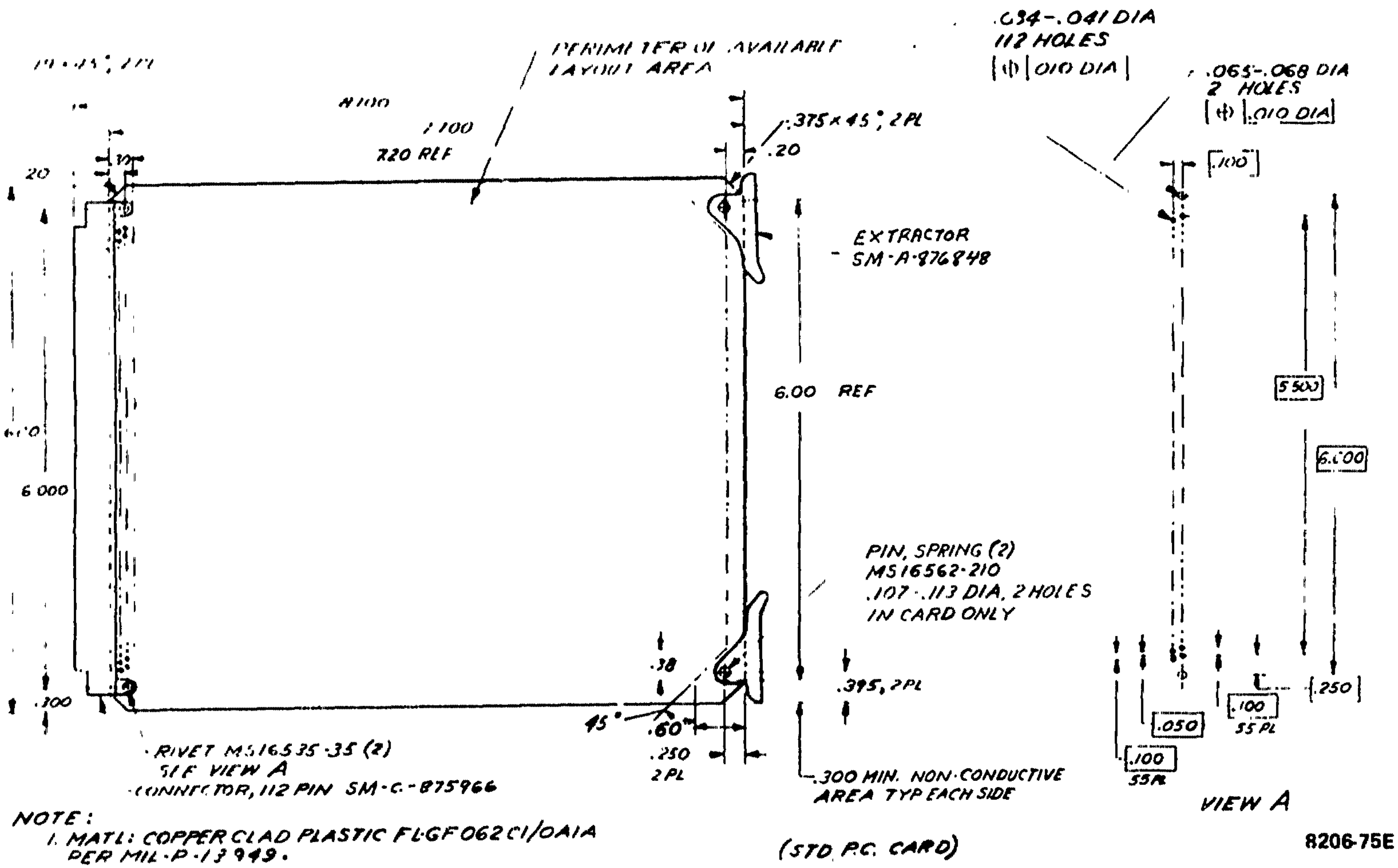


Figure 15-8. Standard Panel

The layers consist of multiple signal layers with inner voltage layer and a ground layer. RMC and RLGM PCB's are not dependent on conduction cooling, resulting in a less sophisticated system.

The alpha-numeric matrix for the location of DIPs which predetermines the location of the DIP to a grid pattern allows adequate space between DIPs for interconnections and discrete components such as diodes, resistors and capacitors while maintaining established locations compatible with automatic insertion equipment, as needed. The standard PCB excluding the connector and extractor has a component and signal area of 43 inches square. The PCBs are designed to meet MIL-STD-275C, and MIL-P-55640 as applicable.

15.4.2.3 Weight

The basic remote equipment case less the electronics weighs approximately 10 kg. The weight of the PCBs average 0.3 kg. Weight breakdowns and total weights for each of the remote units are given in Table 15-5. The RLGM exceeds the specification weight due to a recent increase in the power supply weight. Present estimates show that the RLGM will be about 1.1 kg over the present spec weight.

The weight control effort was fully active. As with any formal weight control activity, the initial action has been to establish bogey weights designed to achieve specification conformance.

TABLE 15-5. RLGM AND RMC WEIGHTS

WEIGHT, KG

Unit	Case Assembly	PCBs	P.S.	Connector/ Wiring	Total Weight	Specification
RLGM	9.6	1.9	4.0	1.1	16.9	15.5
RMC	10.1	3.3	4.2	1.9	20.1	21.2

15.4.2.4 Thermal Design

15.4.2.4.1 General

A thermal analysis of the unit and its modules was used as one of the criteria for part selection. Individual modules and units were breadboarded and temperature tested to insure that the design and parts are compatible with temperatures resulting from the maximum and minimum thermal extremes for the equipment. During the DGM Proposal Phase, preliminary thermal analysis results were used to establish the basic design for the equipments and to select parts/subassemblies. Design techniques which were used are:

a. Use of MIL-Grade, selected components: i.e., 125°C ICs; materials to withstand solar radiation effects and high-low temperature degradations

b. Closed loop convection cooling with direct-to-ambient conduction and convection cooling for PS.

c. Metals and plastics selected for specific proven qualification at extreme low temperature; i.e., polycarbonate used has been recorded serviceable after 24 hour exposures at -80°F

d. Use of silicone rubber seals and gaskets rated not to set at levels as low as -70°F.

15.4.2.4.2 Analysis

The preliminary thermal analyses were updated for the DGM Remote type units in an effort to establish:

a. Thermal guidelines for use in the many tradeoff studies which are in progress

b. Thermal guidelines for use by the mechanical designer in selecting the configuration and the key parts (e.g., card guides) of the subject unit

c. Thermal guidelines for use by the system engineer/circuit designer in "partitioning" the units.

The following thermal summary provides the final status of thermal dissipations and temperatures on remote equipment.

Thermal Summary

There were two major changes in the design path to diminish power dissipations within the remote units.

1. CMOS components will replace most of the low power Schottky ICs to greatly reduce power dissipations in the card nests.
2. Custom designed power supplies with 66% efficiencies which enhanced reduced power supply dissipations.

Power Status: Card nest and power supply dissipations are summarized in Table 15-6. This data is compiled based on design goals of a 66% efficient power supplies. The highest dissipating card is the timing generator at 5.9 watts.

Environment: The environment to which the units are to be exposed is 160°F.

Relevant Design Details: Both units are totally closed with heat sinking in the rear of the power supplies for the RMC unit. There are no heat sinks required for the RLGM. Heat sinking is adequate to dissipate at least 50% of the power supply total dissipation.

TABLE 15-6. POWER DISSIPATIONS

Description	Power	
	RMC	RLGM
Watts Out	52.8	9.6
Watts In Nest	13.5	8.4
P.S. Dissipation	33	9.0
*Total	99	27

*Total power input to power supply (66% efficient power supply).

The card racks are designed in all cases as to provide at least 0.4 inch between PC cards and case skin to promote convection currents around the cards.

Synopsis: Dissipations from each box were broken down into three sections for analysis:

1. Outside skin to ambient dissipation - there is radiation with a 50% view factor from all but the bottom of the boxes. There is also natural convection from all but the bottom
2. Power supply and internal ambient to unit skin dissipation - convection and radiation will be relied upon for this phase of heat dissipation
3. PCB to internal ambient convection dissipation.

Conduction, though not relied on for heat dissipation, renders the above summary conservative.

Results of the thermal analysis are shown on Table 15-7.

TABLE 15-7. WORST CASE THERMAL ANALYSIS RESULTS

	RMC	RLGM
Case Skin Temp	$81^{\circ}C$	$77^{\circ}C$
P.S. Case Temp	$96^{\circ}C$	$85^{\circ}C$
P.S. Transistor Jct Temp	$120^{\circ}C$	$111^{\circ}C$
Max. Allowable P.S. Transistor Jct Temp	$200^{\circ}C$	$200^{\circ}C$
Avg. Temp in Card Nest Area	$90^{\circ}C$	$83^{\circ}C$
Max. Internal Ambient Temp in Card Nest Area	$98^{\circ}C$	$91^{\circ}C$
Max. Allowable Internal Ambient Temp in Card Nest Area	$135^{\circ}C$	$135^{\circ}C$
Max. Card Component Case Temp	$109^{\circ}C$	$103^{\circ}C$
Max. Card Component Jct Temp	$114^{\circ}C$	$107^{\circ}C$
Max. Allowable Card Component Jct Temp	$150^{\circ}C$	$150^{\circ}C$

15.4.2.5 Environmental

Both remote units are designed to the requirements listed on Table 15-8. The most severe of these requirements is rough handling when being transported in the field. This rough handling is simulated by dropping the case 4 feet on each corner, side and face. Acceleration levels in the range of 150 to 200 g's are transmitted to interior components and assemblies.

The primary function of the equipment structure is: (1) to retain the printed wiring boards in such a manner that they will maintain connector engagement and permit unit operation after each of the dynamic tests, (2) to adequately support the power supply, and (3) maintain water submersion integrity after drop. The boards are inserted from the front of the unit within slots in minimum friction guides and engage the connector receptacles in the connector plate. When the front panel is closed, the cards are rigidly retained in all axes.

When the unit is loaded in the vertical direction, the cards are retained by the card guides, which are, in turn, supported by an intermediate structure. The intermediate structure transfers the card and connector plate loads to the front and rear case flanges.

When loading the unit horizontally parallel to the plane of the connector plate, the card loads are taken out through the card connector pins and then into the connector plate. In addition, part of the card loads are transmitted directly to the front panel through the center card retainer.

When a force tending to pull the cards out of the connectors occurs, the upper and lower card retainers mounted on the front panel maintain the card engagement in the connector plate. The card interface is a rubber strip which absorbs tolerances and always maintains positive pressure on the cards. Card loads are distributed by the retainers into the top and bottom edges of the front panel and then to the case flanges.

TABLE 15-8. ENVIRONMENTAL DESIGN REQUIREMENTS

Environmental Condition	Design Requirement	Test Requirement
High	125^{o}F - plus solar operating	Method 501, PROC II 160^{o}F MIL-STD-810
Temperature	160^{o}F Non-operating	Method 501, PROC II 160^{o}F MIL-STD-810
Low	-50^{o}F Operating	Method 502, PROC I - 50^{o}F MIL-STD-810
Temperature	-70^{o}F Non-operating	Method 502, PROC I -70^{o}F MIL-STD-810
Humidity	Tropical level	Method 507, PROC III MIL-STD-810
Altitude	10,000 ft. Operating 40,000 ft. Non-operating	Method 500, PROC I (40,000 Ft. max) MIL-STD-810
Dust	Fine Dust 35 KPH winds	Method 510, PROC I MIL-STD-810
Salt Fog	Salt Sea Atmosphere	Method 509, PROC I MIL-STD-810
Fungus	Fungus resistant	Method 508, PROC I MIL-STD-810
Vibration	Field transport by military vehicles	Method 514.1, PROC XI, Part 2 MIL-STD-810
Shock	Field transport by military vehicles, rough handling	Method 516.1, PROC II MIL-STD-810
Immersion	Leak proof in 3 ft. water	Method 512, PROC I MIL-STD-810
Rain	Heavy precipitation with intermittent wind	Method 506, PROC I MIL-STD-810

When a force tending to push the cards further into the connectors occurs, card loads are taken out by the stiffened connector plate which is in turn fastened to the case flanges. The connector plate stiffeners assure against failure under this loading.

The front of the power supply transmits loads directly into the case flanges for all modes of force. Shear pins which engage the rear of the power supply will transmit horizontal and vertical loads into the case flanges.

The design of the units was proven by extensive detailed structural analyses, a mechanical model testing program, past experience of units utilizing this design at higher loads and 4 foot drops.

As an aid in selecting the present design concept, several structural analyses were performed. To ascertain the space available within the cases, an analysis of the minimum case flange bend radius was performed. This analysis demonstrated that a minimum of 0.54 inches is allowable at the case corners.

Verification of the outside case structure design was demonstrated by mechanical model testing.

In summary, structural designs have been developed which are multi-purpose in nature, i.e., front-to-back, flange to flange stiffening which also acts as P.C. supports/guides; front and rear panels act as covers, retainers, component, connector mounts, as well as case shear panels. This technique enhances weight limiting efforts.

No fixture design was required for the remote units. Shock testing consisted of a 4 foot drop on to a 2 inch plywood floor, while vibration consisted of an unrestrained bounce test on a package tester capable of performing bounce testi..g per MIL-STD-810.

The Humidity Test was conducted to determine the resistance of the units under exposure to a warm, highly humid atmosphere such as is encountered in tropical areas. The principal areas of concern in designing to withstand humidity were component selection and breakdown between closely spaced electrical interconnections. The selected panel components are all sealed for protection against the environment. All Printed Circuit Board components and interconnections are protected with a polyurethane coating per MIL-I-46059. This coating has been successfully tested on many previous prlgrams. The mechanical design assures against moisture entrapment that could degrade electrical performance by using vertically oriented interconnections for the printed circuit cards and their associated wiring.

The Rain Test was performed without the protection of the equipment case covers, and the unit was operated during the test. After the test, the unit was operated. To assure sealing the case openings, the mating panels are flange-mounted to the case with a neoprene-gasketed interface that provides a rain seal. Tiedown hardware is spaced to assure adequate compression of the gaskets. In addition, each individual panel component is mounted with a weather gasket, thus sealing all panel openings. Further, all components on the panel are qualified for operation in a rain environment.

The units are both capable of immersion to a covering depth of three feet of water for two hours without leakage. This was accomplished by a base design that incorporates rigid tongue and groove interfaces having O-Ring gasket seals. The gaskets are compressed by cam action latches. The pressure relief valve is the only other case opening. This opening is protected against leakage by establishing a differential operating pressure in excess of that which occurs during the Immersion Test.

The case seals which were provided for the Immersion Test also prohibit the entrance of sand and dust. The units in operating configuration are also protected from sand and dust by the same seals that protect against the rain environment. There are no exposed areas that could entrap dust particles and degrade operation.

The units are resistant to the corrosive effects of extended exposure to a salt-sea atmosphere. This is accomplished by material and component selection and proper application of corrosion resistant finishes. For example, all aluminum parts were coated per MIL-C-5541.

The units use only fungus-resistant grades of materials, in accordance with Requirement 4 of MIL-STD-454. The materials do not provide nutrients or support fungus growth. Special attention was directed to the selection of adhesives, film materials, and plastic components.

The Altitude Test was conducted to determine the effects of reduced pressure on the units. Reduced air pressure resulting from air transportation at altitudes up to 40,000 feet above sea level was considered in the Case Design.

Both cases are equipped with pressure relief valves designed to prevent large pressure differentials which could cause structural damage. The relief valve opens at a pressure differential of three psi. Pressure differentials of up to three psi were considered in the design of the cases and do not cause damage. The relief valve also can be operated manually to negate small negative pressure differentials which may inhibit removal of the transit covers.

All components used in the units are capable of exposure to altitudes of 40,000 feet without degradation of their operating characteristics.

Unit operation at 10,000 feet altitude simulates conditions found at high ground elevations. All components operate at this altitude without any degradation of performance.

15.4.2.6 EMI Design

15.4.2.6.1 General - The remote equipment is designed to meet the applicable requirements of MIL-STD-461. An EMP filter is integrated into the power supply case. The output of the EMP filter is connected to a power line filter within the power supply. All access covers, power supply front panel, connectors and external mounted components are gasketed and/or electrically and mechanically bonded to control RFI. Conductive finishes were selected from MIL-F-14072. The units were designed and constructed with adequate provisions for bonding the unit to a subsystem ground plane. Bonding is not accomplished through screws connecting the equipment to mounting racks. Bonding jumpers are of the solid metal type and are as short as possible. However, in no case is the length to width ratio of the jumper in excess of 5 to 1. Bonding techniques employed do not impede maintainability nor adversely affect interchangeability. Surfaces being bonded together are prepared by removing all anodic film, grease, paint, lacquer, dirt or other foreign and high resistance materials or agents from the immediate area to insure negligible rf impedance between the adjacent metal parts. Upon completion of the bonding assembly and ascertainment of the specified 2.5 milliohm bonding impedance, the completed assembly was refinished in accordance with MIL-F-14072. All panel mounted connectors and components and the panel mating surfaces are free of non-conductive finishes and provide positive bonding and grounding with mating connectors and equipment ground plane. The bonding dc resistance of all connectors and panel mounted components does exceed 2.5 milliohms.

The gasketing systems employed for the remote equipments required rain seals and therefore, uses EMI/weather proof seals. The cover over the PCB's and the power supply front panel features gasketing with controlled compression stops to maintain proper conductive sealing. The rear access

panel over the W/W plate is EMI protected, as is the rear protrusion of the power supply. Captive hardware is located around the periphery of the covers and panels spaced to provide adequate RFI compression without causing unnecessary hardware removal to gain access to the subassemblies for replacement. A summary EMI design is outlined in the following paragraphs.

15.4.2.6.2 EMI Envelope - The outer surface of each unit was defined as the EMI envelope for design purposes. Each unit housing was designed and constructed to provide the required shielding effectiveness. The impedance between any two points on the housing is constant and as low as possible at any frequency. This was accomplished by using highly conductive mating surfaces, close mechanical tolerances, and rigid construction.

15.4.2.6.3 Grounding - Each unit utilizes a multi-point ground, i.e., all signals within the unit are referenced to a large, easily accessible, low impedance surface area, specifically, the equipment housing. This type of grounding scheme minimizes common impedance sharing between circuits and provides maximum effectiveness from filters, shields, and decoupling networks. Certain high level currents within the system are routed through return wires as required. Each unit is provided with a power safety ground through its I/O connectors. Bonding impedances are less than 10 milliohms measured at dc.

15.4.2.6.4 Ventilation - Forced cooling air, internal to the unit, was not used. Closed loop convection internal cooling was employed. Therefore, EMI integrity was not compromised due to cooling requirements.

15.4.2.6.5 Printed Circuit (PC) Boards - PC boards with ground planes and more than three chassis ground connections are far superior to those with grounds which are interspersed among the interconnecting etches. The ground plane minimizes common impedance sharing between circuits on the board and also acts as an RF shield to reduce board-to-board coupling. When multilayer PC boards are used, a ground plane is a practical necessity, and was used.

15.4.2.6.6 Internal Wiring - In an equipment which processes only digital signals. the internal wiring arrangement is less critical, since practically any configuration will be adequate. However, when an equipment processes digital, analog, and high-level continuous wave (CW) signals, the layout becomes critical because of coupling within the wire harnesses. The two factors which reduce cable coupling are use of shielded cables which are properly terminated, and physical separation. These techniques were used in the design of all the DGM units.

15.4.2.6.7 Switches and Indicators - All external switches utilize grounded shafts. Indicators are shielded.

15.4.2.6.8 Power Supplies - Power supply noise and operational signals at the power supply input are reduced to the lowest possible levels through design. This results in lower insertion losses for the power-line filter, which reduces filter size and cost. A solid-grounding approach helps reduce power supply noise.

15.4.2.6.9 Filter Installation - There are two major criteria involved with filter installation. First, the output wires must be isolated (shielded) from the input wires by at least the insertion loss of the filter. Second, the case of the filter must be referenced to the same ground point as the signals it will attenuate: that is, the RF impedance between the installed filter and the signal reference must be as close to zero as possible. This type of filter installation was used as it achieves maximum insertion loss from the filter.

15.4.2.6.10 Access Panels - Panels, as described, were held to a minimum with least peripheral length to complement EMI seal.

15.4.2.6.11 RF Gaskets - For maximum shielding effectiveness, a gasket must mate with clean and rigid surfaces, must have resiliency, and must be uniformly compressed more than 50 percent. Therefore, screw spacing for the mating surfaces was selected in accordance with Figure 15-3.

15.4.2.6.12 Required Shielding Effectiveness - Each unit enclosure is designed to provide 60 dB of shielding effectivesness. This provides sufficient attenuation to reduce all radiated signals to levels below the MIL-STD-461A

and Tempest limits. Views of the outer cases are integrated in Figures 15-5 and 15-6. The basic frame is of welded construction. The front and back covers were sealed with an RF gasket and bolted into place. All gasket mating surfaces were finished with irridite to prevent corrosion, but this finish did not degrade the shielding effectiveness as the gasket bites into the frame when the covers are secured.

15.4.2.7 Power Supply

The power supply was designed as a separable plug-in subassembly mating with rack and panel style connectors at the rear and mounting via captive hardware at the front of the equipment case. The RMC incorporates a finned (heat sink) rear panel on the power supply, protruding through a gasketed opening in the case rear panel. Design of the fin assembly required that 50% of the Power Supply dissipation transfers directly to outside ambient at a minimum. Closed loop convection was utilized for the balance. Figure 15-9 shows the P.S. configuration. The RLGM did not require a heat sink due to its relatively low power characteristic. However, all supplies including those for the shelter unit (LGM) use common subassemblies. The general construction is accomplished by use of a machined plate seam type of enclosure.

The power supply houses four modules (as listed in Table 15-9). Each module is a plug-in type of P.C. board. The major heat dissipating component in the RMC boards is mounted on a metal heat sink which is an integral part of the board assembly. These heat sinks are mounted to the finned heat sink on the unit by hardware which is accessible from the rear of the power supply. Since the RLGM does not have a heat sink or high heat dissipating component, the heat sinking feature was not required. The front edge of all boards is secured by a card guide. Both the upper and lower edges of the board are held in place by retaining bars. The front compartment provides clearance for front panel components. Some components are also mounted directly to the case structure.

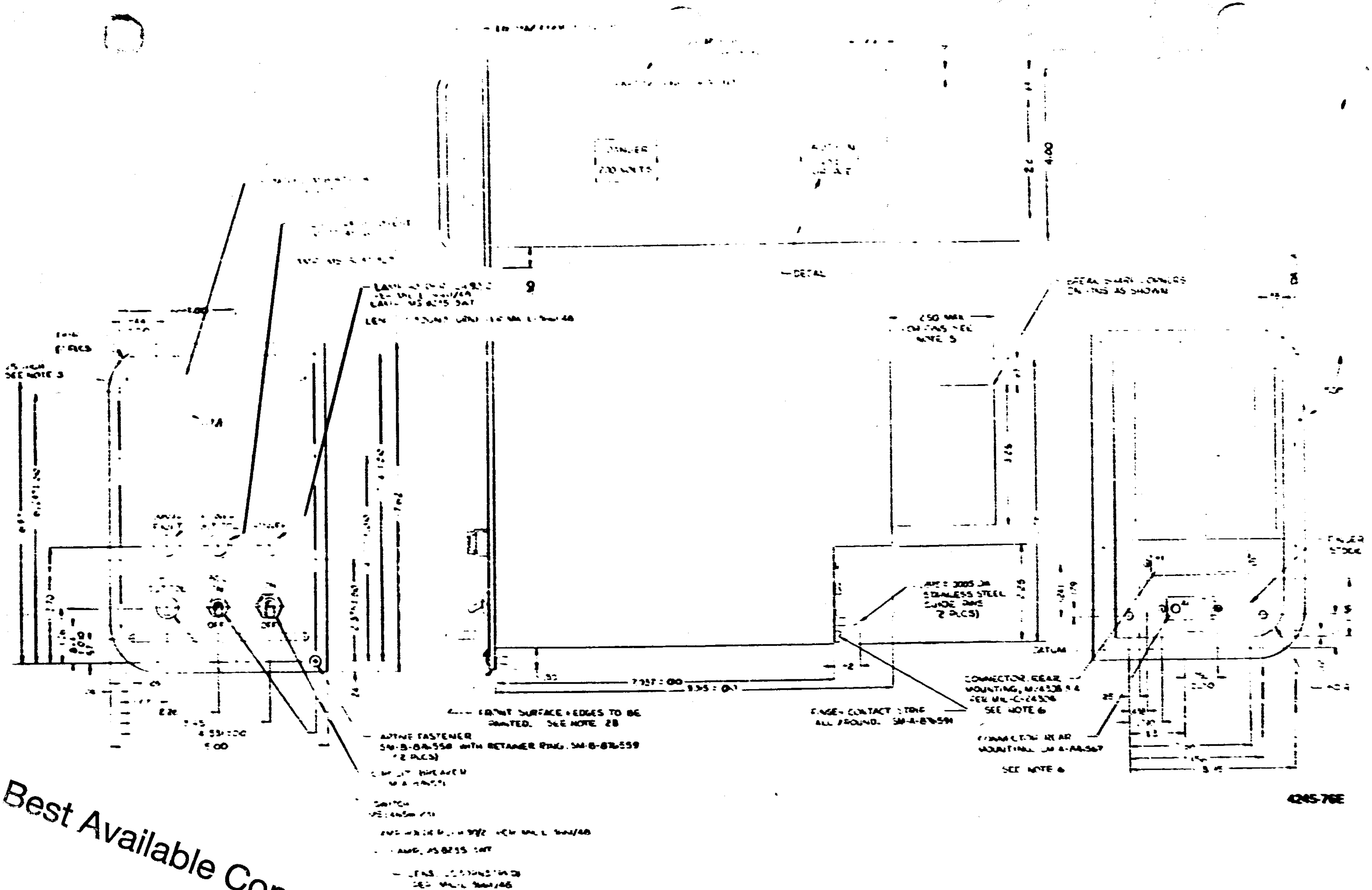


Figure 15-9. Power Supply

TABLE 15-9. RMC AND RLGM POWER SUPPLY ASSEMBLIES AND ALLOCATIONS

		RMC	RLGM
1.	(B Module)	1	1
2.	(C Module)	1	1
3.	(D Module)	1	0
4.	(H Module)	0	1
5.	(J Module)	1	1

The overall P.S. unit as noted earlier is serviceable as a sub-unit from the front of each remote unit. A system of guide tracking is provided to allow for direct insertion of the supply into the RMC or RLGM. Shock blocks and pin engagement provide the mechanical interface at the rear with positive automatic engagement of the rear connectors. As the engagement is accomplished, the supply is lifted by the tapered shock block pins off the unit slide track. The front panel fasteners then accomplish the final mechanical lock.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER CORADCOM 75-0036-F2	2. GOVT ACCESSION NO. A088 352	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) Digital Group Multiplexers Vol 2 of 2		5. TYPE OF REPORT & PERIOD COVERED Final - May 1975 - Feb 1980
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) William Hatton, Charles Onthank (Syl.), Paul Graves (Syl.)		8. CONTRACT OR GRANT NUMBER(s) DAAB07-75-C-0036
9. PERFORMING ORGANIZATION NAME AND ADDRESS Raytheon Co. Equipment Division Communication System Lab, Sudbury, MA 01776		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 28010A 1X028010D111 00 011 C31E256 C8 CSC
11. CONTROLLING OFFICE NAME AND ADDRESS Project Manager Multi-Service Communication Systems, Fort Monmouth, NJ 07703		12. REPORT DATE Feb 1980
		13. NUMBER OF PAGES 225
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) CORADCOM/CENCOMS Signal Processing Division DRDCO-COM-RF-1, Fort Monmouth, NJ 07703		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for Public Release: Distribution Unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

There are two volumes to the report.

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Multiplexing	Phase	Reliability	Filters	Humidity
Modems	Repeaters	Logic	Amplifiers	
Telemetry	Cable System	Assembly	Power Supplies	
Frames	Circuit	Scanner	Shock	
Frequency	Buffers	Bipolar Systems	Vibration	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The technical objective of this program was to develop a family of Digital Group Multiplexers (DGM) which form an integral part of the communications Nodal Control Element (CNCE) and the Transmission Facilities associated with the Automatic Central Office Communications, AN/TTC-39 (Automatic Switch). The DGM consists of 13 different equipments which 3 are mentioned in this technical document. These are Loop Group Multiplexer (LGM), Remote Loop Group Multiplexer (RLGM), and the Remote Multiplexer Combiner (RMC).

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

20. (Continued)

The multiplexers and cable transmission equipments will be employed primarily in technical communications control facilities to serve clusters of digital subscribers in a switched network and to provide digital transmission to to Radio Park Via radio or cable.